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# Vermessung von ADC Nichtlinearitäten und Entwicklung eines Bias Boards für den TRISTAN Detektor / Measurement of ADC Nonlinearities and Development of a Bias Board for the TRISTAN Detector

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# List of Abbreviations

| | |
|---|---|
| ADC | Analog to Digital Converter |
| DAQ | **D**ata **A**c**Q**uisition system |
| DNL | differential nonlinearity |
| FPGA | Field Programmable Gate Array |
| FWHM | full width half maximum |
| IIR | infinite impulse response |
| INL | integral nonlinearity |
| JFET | Junction Field Effect Transistor |
| LSB | least significant bit |
| PCB | printed circuit board |
| PDF | probability density function |
| SDD | Silicon Drift Detector |
| TRISTAN | **TR**itium **I**nvestigations on **ST**erile to **A**ctive **N**eutrino mixing |
| WGTS | Windowless gaseous tritium source |

# Chapter 1.

# Abstract

The KATRIN experiment is currently the most precise experiment neutrino mass measurement, from tritium $\beta$-decay. To this day the KATRIN collaboration has determined an upper mass limit on the effective neutrino mass $m(\nu) < 0.8\frac{eV}{c^2}$ (at 90 % C.L.) [4]. With this uniquely precise expeirmental setup it's possible to search for a sterile neutrino in the mass range of several keV, a viable dark matter candidate. To start the search, the KATRIN experiment will be upgraded with the new TRISTAN detector, a precision, low noise silicon drift detector capable of handling $\beta$-decay electron count rates of up to $10^5$ electrons per second. In the KATRIN setup, the detector will be located in a strong magnetic field, requiring magnetic field compatible electronics for biasing and readout.
The goal of this work was to develop schematics for a magnetic field compatible bias and readout system, which can be used for the final TRISTAN setup. I designed, build and tested these schematics, which showed good performance. I also identified the design weaknesses, which can be improved in the next hardware iteration.
In the first part of the thesis I will introduce the KATRIN experiment, follow up with the electronic signal chain of the TRISTAN detector, and continue with the requirements and design of the bias and readout electronics.
With the built electronics I sucessfully operated our prototype detector, which allowed me to compare the existing, non magnetic field compatible setup with the thesis setup. At last I discuss the results and improvements to be made.
In the second part of this thesis I explain the histogram technique of measuring and evaluating nonlinearities of the analog to digital converter, a critical component in the signal chain, which could introduce distortions into the measured signal and potentially create a false sterile neutino signal. Therefore these nonlinearities need to be precisely known and accounted for.

# Chapter 2.

# Neutrino Physics

## 2.1. Discovery

Wolfgang Pauli postulated the neutrino in 1930, after in the year 1914, electron energy spectra of $\beta$-decays have been observed to be continuous. In the process of $\beta$-decay, a neutron within a nucleus decays into a proton, an electron and an electron antineutrino, as shown in equation 2.1

$$n \rightarrow p + e^{-} + \nu \tag{2.1}$$

If hypothetically the $\beta$-decay only involved the decaying nucleus and the electron itself, the the electron energy spectrum would be mono-energetic, as it's defined by momentum conservation. The observation of the continuous spectrum led Pauli to the conclusion that a third particle must be involved, which had to be very light, without charge, and very weakly interacting. The low mass and the tiny interaction cross section of the neutrino makes experiments notoriously hard, often requiring large experiments, with very huge detectors.

## 2.2. Neutrino Properties

Neutrinos are uncharged elementary particles with spin ½, and to our current knowledge interact only via the electroweak force and gravity. Each neutrino has a negatively charged partner of their flavor, there are: electrons ($e^{-}$) and the electron neutrinos ($\nu_e$), muon ($\mu^{-}$) and muon neutrinos ($\nu_\mu$)
and taus ($\tau^{-}$) and the tau neutrinos ($\nu_{tau}$).
The Standard Model of particle physics states that neutrinos are mass-less particles, but experiment show otherwise. The most recent and advanced experiments, including the SNO Experiment [25] and SuperKamiokande [16], show that the neutrinos oscillate from one type to another, changing flavor. The Standard Model of particle physics does not have any explanation for this process. Therefor the scientists Pontecorvo, Maki, Nakagawa and Sakata developed the PMNS theory, stating that neutrinos interact in their flavor states, but propagate in their mass eigenstates, noted as $|\nu_1\rangle, |\nu_2\rangle, |\nu_3\rangle$. The connection between the flavor eigenstates and the mass eigenstates is given by the unitary PMNS matrix, shown in 2.2. The matrix elements $U_{i,j},\ i \in \{e, \mu, \tau\},\ j \in \{1, 2, 3\}$ are transition probabilities from mass eigenstate to flavor eigenstate. The relative phase of each mass eigenstate evolves with time, so when the neutrino decides to interact with matter, the probability to find it in a certain flavor changes with time.

$$\begin{pmatrix} |\nu_e\rangle \\ |\nu_\mu\rangle \\ |\nu_\tau\rangle \end{pmatrix} = \begin{pmatrix} U_{e1} & U_{\mu 1} & U_{\tau 1} \\ U_{e2} & U_{\mu 2} & U_{\tau 2} \\ U_{e3} & U_{\mu 3} & U_{\tau 3} \end{pmatrix} \begin{pmatrix} |\nu_1\rangle \\ |\nu_2\rangle \\ |\nu_3\rangle \end{pmatrix} \tag{2.2}$$

How heavy these mass eigenstates are, has been a topic of research since more than 50 years. The observable mass of a flavour eigenstate is then given as the incoherent sum of the three neutrino mass eigenstates. For the electron neutrino $\nu_e$, the observable mass is shown in equation 2.3.

$$m(\nu_e) = \sqrt{\sum_j^3 |U_{ej}| m_j^2} \tag{2.3}$$

From neutrino oscillation experiments, it's only possible to determine the difference of the squared mass-eigenstates, with $\delta m_{21}^2 = m_2^2 - m_1^2$, without direct clue on the mass ordering. The sign of the $\delta m_{21}^2$ mass splitting is known due to the Mikheyev - Smirnov - Wolfenstein effect, and is $m_{21}^2 = (7.53 \pm 0.18) \times 10^{-5} \mathrm{eV}^2/\mathrm{c}^4$ . The value of the mass splitting, $\delta m_{32}^2$ value, depends on the ordering of the neutrino masses. For normal ordering with $m_1 < m_2 < m_3$, $\delta m_{32}^2 = 2.54(2.51 \pm 0.05) \times 10^{-3} \mathrm{eV}^2/\mathrm{c}^4$, and for $m_3 < m_1 < m_2$, $m_{32}^2 = (-2.56 \pm 0.04) \times 10^{-3} \mathrm{eV}^2/\mathrm{c}^4$ [6].

## 2.3. Limits on Absolute Neutrino Mass

The upper neutrino mass limit from cosmological models currently provide the most stringent upper mass limit on the sum of all three neutrinos ($\sum m_\nu < 0.12$ eV/c$^2$)[2], by combining datasets from gravitational lensing and baryonic acoustic oscillations measurements. This value depends on the correctness of the ΛCDM model, which was assumed for the data evaluation. The KATRIN Experiment allows a precise, model independent measurement of the effective neutrino mass.

**Mass Measurement via the $0\nu\beta\beta$-decay** The neutrinoless double beta decay $0\nu\beta\beta$, is a second order, lepton number violating decay mode that requires two simultaneous beta decays, where theoretically both neutrinos of the beta decay annihilate with each other. This decay would require neutrinos to be Majorana particles and therefore their own antiparticle. The decay equation of a nucleus with a proton number Z and the mass number A would be

$$(Z, A) \rightarrow (Z + 2, A) + 2e^-$$

instead of two independent beta decays, where two neutrinos would be produced.

$$(Z, A) \rightarrow (Z + 2, A) + 2e^- + 2\bar{\nu}_e$$

The mass of the neutrino can be derived from the decay half life time. Albeit extensive search, an evidence of a $0\nu\beta\beta$ decay has not been found. The currently best limit for the half life time of the $0\nu\beta\beta$ decay is $T_{1/2} > 1.810^{26}$ yr from the GERDA collaboration [3]. Hence, the limit on the effective Majorana neutrino mass would be $m_{\beta\beta} = \left|\sum_{i=1}^3 U_{ei} m_i\right| < 79 - 180$
$mathrm\ meV/\mathrm{c}^2$.

## 2.4. Sterile Neutrino

The sterile, right-handed neutrino is a minimal extension to the Standard Model and would be a possible dark matter candidate [27]. It is called sterile because it would not even interact via the electroweak force, but only via mixing with the left-handed neutrinos, therefore being extremely hard to detect. Right handed sterile neutrinos can

generate the mass of usual neutrino, by adding a Majorana mass term to the Standard Model Lagrangian. Through the see-saw mechanism sterile neutrinos could explain the lightness of the standard model neutrinos. This postulated sterile neutrino mass could be in the $\mathcal{O}$(keV) range, which would be detectable with the KATRIN experiment. An imprint of the sterile neutrino would be visible in a kink-like structure on the differential tritium decay spectrum as shown in figure 2.1. With a sterile neutrino, the differential spectrum consists of the active neutrino spectrum $\frac{\mathrm{d}\Gamma(m_a)}{\mathrm{d}E}$, with an admixture of the sterile neutrino $\frac{\mathrm{d}\Gamma(m_s)}{\mathrm{d}E}$. The angle $\theta$ describes the strength of mixing.

$$\frac{\mathrm{d}\Gamma}{\mathrm{d}E} = \cos(\theta)^2 \frac{\mathrm{d}\Gamma(m_a)}{\mathrm{d}E} + \sin(\theta)^2 \frac{\mathrm{d}\Gamma(m_s)}{\mathrm{d}E} \tag{2.4}$$

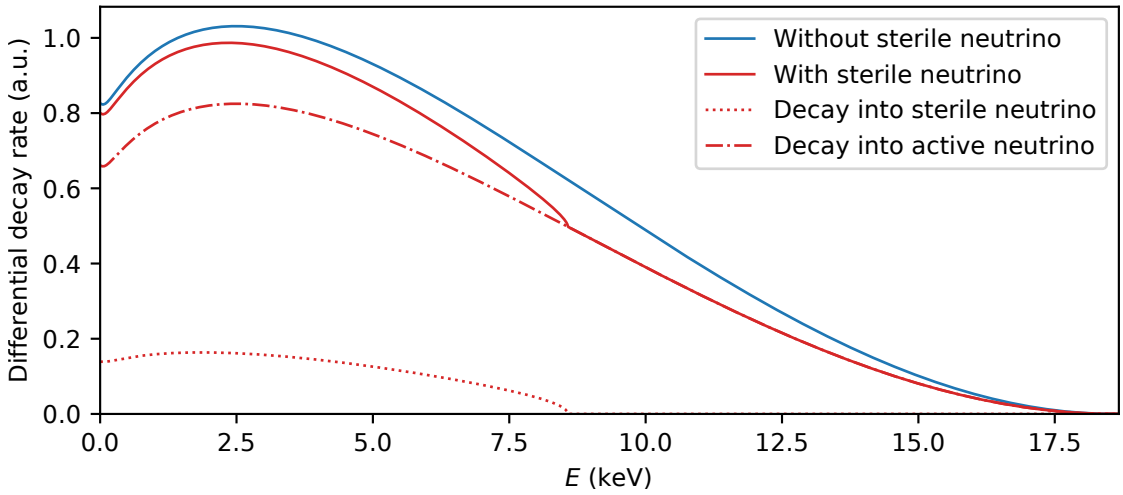



**Figure 2.1.:** A model for tritium decay an unphysically strongly interacting sterile neutrino, showing the kink like structure, the KATRIN Experiment is looking for [33].

# Chapter 3.

# The KATRIN Experiment

The main goal of the KATRIN experiment is to measure the effective mass of the electron anti-neutrino. This is accomplished by measuring the electron energy at the endpoint of the $\beta^-$-decay spectrum, as shown in figure3.1. The difference between $E_0$ and the measured electron energy $E$ is the effective anti-neutrino mass.

### 3.0.1. Experimental Setup

With the experimental experience from prior neutrino mass measurement spectrometer experiments, including the Mainz [19] and the Troitsk [1] experiment, KATRIN has been designed and build with an excellent neutrino mass sensitivity in mind, a projected 0.2 eV (at 90 %CL) after a total of 5 years of measurement time. [17]. The main improvements to prior setups are: the ultra stable high activity tritium source [18, 20, 15]; extremely precise high voltage monitoring at the ppm level [7]; and simulations and measurements to determine the spectral energy distortion caused by electrons passing through the gaseous tritium source, and the spectrometers [5].
The coarse experimental setup is shown in figure 3.2. The electrons, radiated from the windowless gaseous tritium source (WGTS) are guided through the differential and the cryogenic pumping section with the use of strong magnetic fields. Those pumping sections are responsible for reducing the tritium rate into the spectrometers by 14 orders of magnitude [23]. Tritium in the spectrometer would increase the background electron signals, and distort the measurement. The electrons, undisturbed by the pumping sections fly into the spectrometer sections, where the first spectrometer filters out the

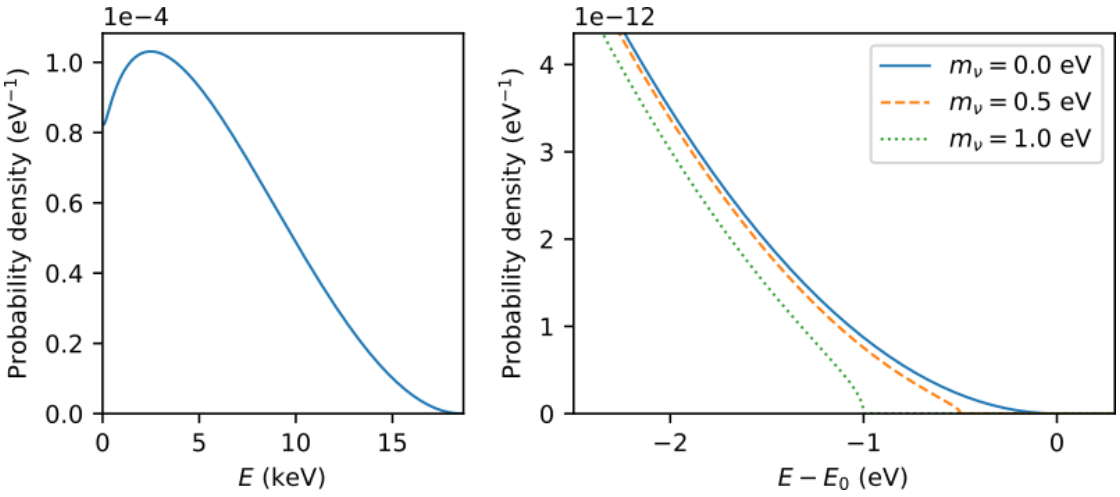



**Figure 3.1.:** (Right) shows an exemplary tritium spectrum. (Left) shows the zoomed -in section of the endpoint at with $E_0 = 18.575$ keV. The spectra are idealized, not taking any experimental effects into account.

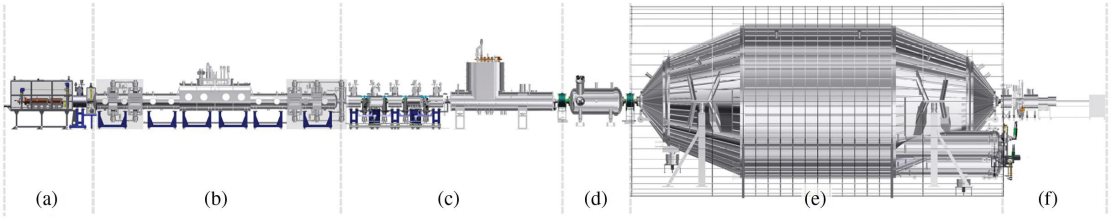



**Figure 3.2.:** The major components of the KATRIN beam line consist of (a) the rear section for diagnostics and control of the plasma potential, (b) the windowless gaseous tritium source WGTS, c) the differential pumping section and the cryogenic pumping section, (d) the smaller pre-spectrometer followed by (e) the larger main spectrometer with its surrounding air coil system. This system transmits only the highest-energy $\beta$ decay electrons onto (f) the solid-state detector where the electrons are counted. [17]

most low energy electrons, and leaves only the last fraction of high energy electrons to be filtered by the main spectrometer. With this technique, background radiation is further reduced, as a decreased electron density reduces any secondary effects within the main spectrometer.
Electrons with an energy above the retarding potential pass the main spectrometer and reach the detector, where they are counted.

### 3.0.2. Working principle of the MAC-E Filter

The main spectrometer is a MAC-E Filter, a **M**agnetic **A**diabatic **C**ollimation combined with an **E**lectrostatic Filter. Throughout the experiment, the electrons are guided by a magnetic field, from the source to the detector. The electrons perform a cyclotron motion around the magnetic field while traveling. The filtering is done with a static electric potential – the retarding potential – which is provided by applying a precise high voltage to a wire setup within the spectrometer tank. Only electrons which have a kinetic energy above the retarding potential can pass the potential barrier and hit the detector. In order for the electrostatic filter to work, it's necessary to transfer all of the momentum of the cyclotron motion into motion anti-parallel to the retarding electric field. This is achieved by gradually decreasing the magnetic field density from $B_{max}$ to $B_A$, where the 'A' stands for 'Analyzing Plane'. The energy uncertainty $\Delta E$ of the MAC-E filter depends on how well the cyclotron momentum gets 'straightened out'. This in turn depends on the ratio of $\frac{B_A}{B_{max}}$, leading to:

$$\frac{\Delta E}{E} = \frac{B_A}{B_{max}}$$

So in order to achieve a very good energy resolution, it's necessary to decrease the magnetic field by many orders of magnitude. This is the reason why such a huge spectrometer tank is needed. The whole process of electron filtering is depicted in figure 3.3.

### 3.0.3. Modes of Operation for the Sterile Neutrino with the KATRIN Experiment

The usual operating mode of KATRIN is to set the filter near the endpoint of 18.575 keV, and count the incoming electrons. This mode is called integral mode, as this counts

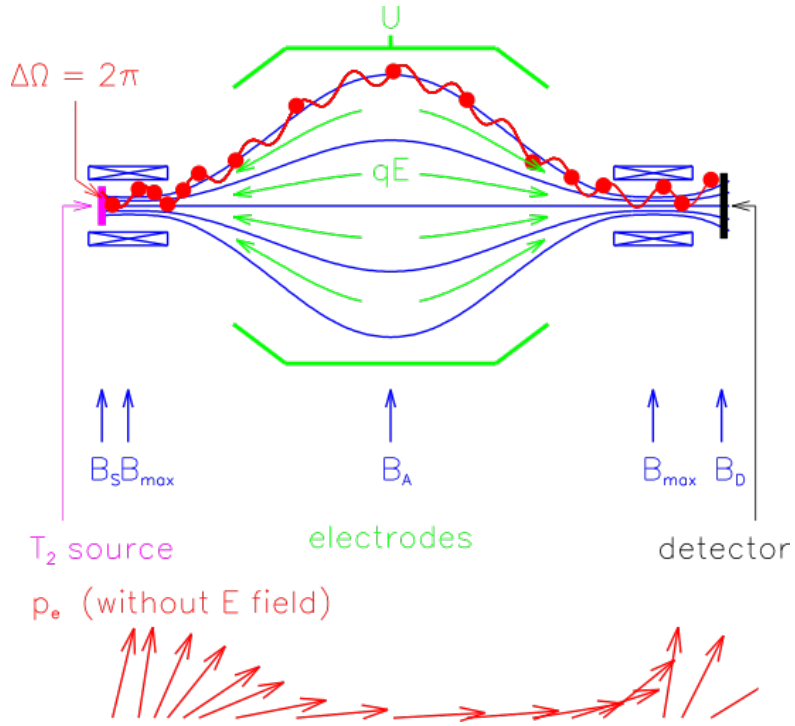



**Figure 3.3.:** Schematic of the spectrometer tank. Blue lines indicate magnetic field, whereas their proximity indicates the magnetic field intensity. The red line indicates a projection of the electron cyclotron path. The red arrows below show a the momentum transfer that goes parallel to the magnetic field lines and perpendicular to the retarding potential. Green lines indicate the electric field. [10]

the electrons between the retarding potential $U_r$ and the endpoint $E_0$ of the spectrum:

$$\Gamma(m_\beta) = \int_{U_r}^{E_0} \frac{\mathrm{d}\Gamma(m_\beta)}{\mathrm{d}E} \mathrm{d}E$$

With this mode it's not possible to search thoroughly for a sterile neutrino kink, deep into the spectrum, as background noise and rate dependent systematic uncertainties distort the measurement [9][p.159].
To get around this limitation, it's necessary to measure the electron energy at the detector, directly recording a differential spectrum. This measurement mode is called differential mode, and requires a detector with an electron energy resolution better than 500 eV, to have a chance to measure a sterile neutrino mixing down to $\sin^2(\theta) > 10^{-8}$ (at 90% C.L.) [24]. In combination with tests, which inject electrons of known energy into the spectrometer is further possible to verify the experimental integrity of the setup, and therefor potential results of sterile neutrino imprints.

## 3.1. The Detector Upgrade TRISTAN

In order to measure the electron energy at the detector, a detector upgrade is required. The newly designed TRISTAN (**TR**itium **I**nvestigations on **ST**erile to **A**ctive **N**eutrino mixing) detector is designed to handle count rates of $\Gamma < 3.4e8$ cps, to measure the whole differential spectrum at a WGTS source strength 1/100 of it's nominal value. The TRISTAN detector operates on the SDD (Silicon Drift Detector) technology, developed in cooperation with the semiconductor laboratory of the Max Planck society (HLL). It is a pixelated detector, build from 21 modules, each carrying 166 pixels. This way the

count rate at every pixel reaches a maximum value of $10^5$ cps.

## 3.2. Working Principle of the Detector

The detector is an improved PIN diode, a diode with a **p**-doped section, a non doped section (**i**ntrinsic semiconductor) and a **n**-doped section. With a very thin, p-doped entrance window, the incoming electrons bypass the entrance window, hit the intrinsic silicon, deposit their energy and create a charge cloud, which is proportional to the energy of the electron. With an electric field across the reverse biased PIN-diode, the charge drifts towards the n-doped anode and gets collected there. In comparison to a simple PIN diode, the SDD uses a very small anode capacitance of 180 fF [21], improving the resolution of the detector. The smaller the anode capacitance is, the better the resolution of the detector, as the capacitance has a quadratic influence on the spectral noise power density of the output signal [26]. Silicon drift-rings on the back side of the detector create a rotationally symmetric electric field within the detector, and drive all the charge within the detector to the anode. The electrons arrive at the anode and create a step like signal, which is amplified by n-JFET integrated on the SDD. The drift ring arrangement of one pixel is shown in figure 3.5. Figure 3.4 shows a prototype 7-pixel detector, which we

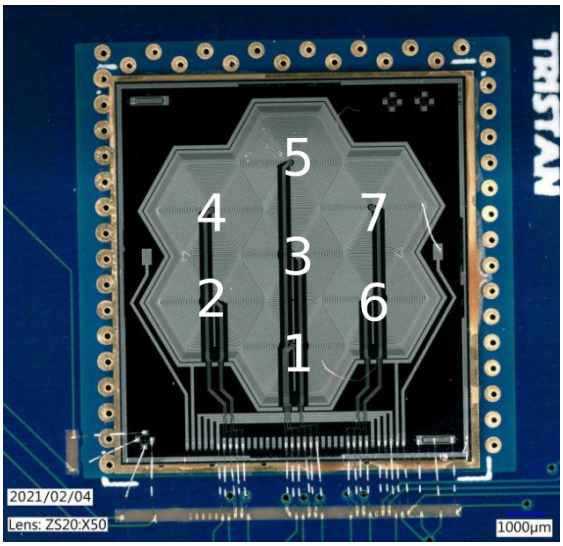



**Figure 3.4.:** The prototype 7 pixel TRISTAN detector used for characterization measurements.

used to perform characterization measurements. With the JFET being on the detector, following amplifier stages can be further away from the detector, which simplifies the electrical wiring for the 3486 pixels. The integration of the JFET allows for a very good energy resolution. With x-rays of a $^{55}$Fe source a resolution of 140eV (FWHM) was reached when the detector was cooled [22]. A prior prototype, without integrated JFET measured 20keV electrons with a resolution of up to 260eV [28].

## 3.3. The Detector Signal

The signal from the detector is shown in figure 3.6. It is a continuously rising ramp with steps, which indicate that particles deposited their energy in the detector. The height of these steps is proportional to the energy deposited in the detector. A zoomed-in version

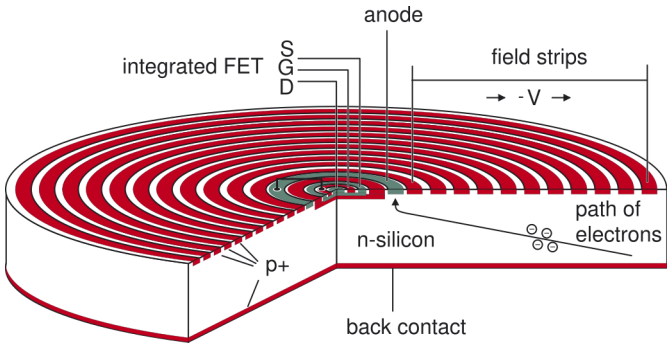



**Figure 3.5.:** Model depicting the SDD. On the bottom of the picture (back contact), the electrons enter the detector and create a charge cloud within the intrinsic silicon layer. The electric field created by the drift-rings (red rings on top) guides the charge cloud towards the gate of the n-JFET, and gets collected [22].

of three events at the detector is shown in figure 3.7. The main ramp comes from leakage current within the detector. The leakage is temperature dependent, and can be reduced by cooling down the whole detector.
As all electronic devices have a specified voltage input range, the ramp cannot rise indefinitely. So the charge on the detector capacitor needs to be flushed with a dedicated reset pulse, which sets back the ramp to the starting point.

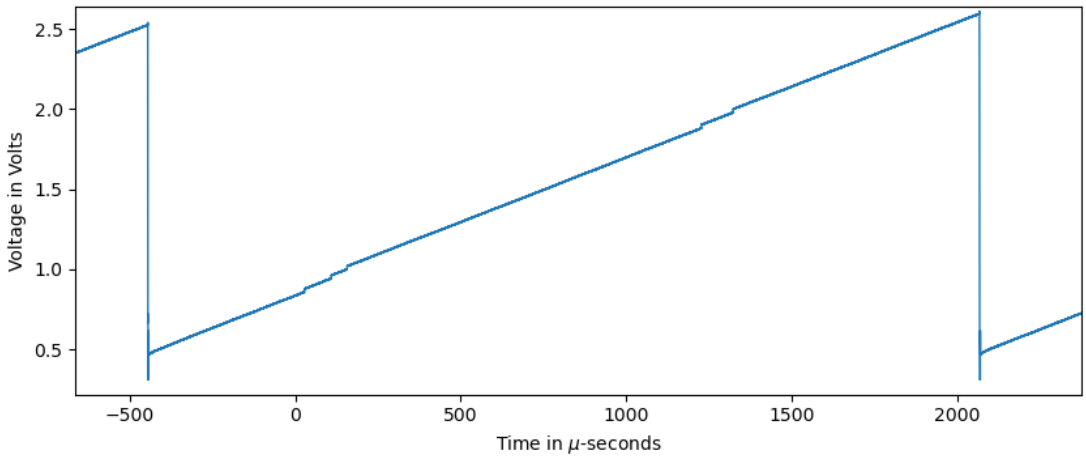



**Figure 3.6.:** The image shows the ramp, one reset on the right, and one on the left. The small step in the ramp are x-ray events.

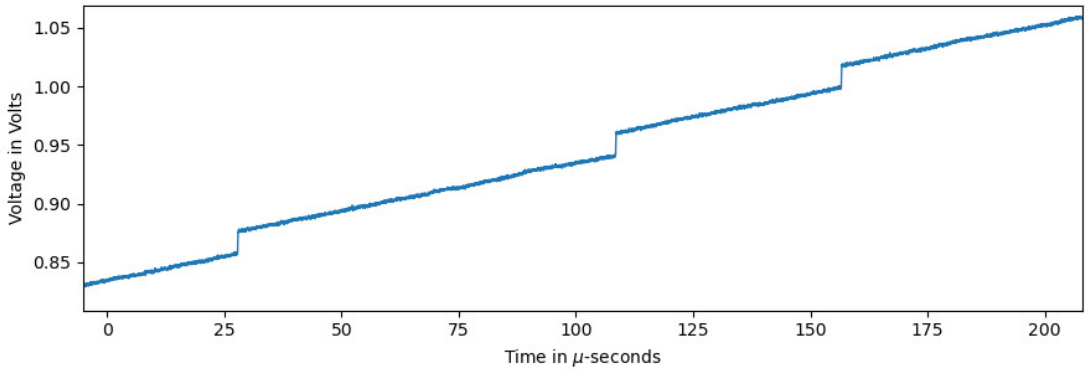



**Figure 3.7.:** The image shows the signal, with three x-ray events in it. The event amplitudes are from 5.9keV x-rays from a radioactive Fe55 source. The leakage current increases with temperature. To reduce the effect of the leakage current, the TRISTAN detector will be cooled.

# Chapter 4.

# The Signal Chain

## 4.1. Overview

In the following, the 'signal chain' means all the hardware and the electronic components involved, from detector signal to the point of first signal processing. A particle arrives at the detector, which generates a small electronic step. This step is then amplified in several stages. The amplified signal arrives at the ADC (Analog to Digital Converter) and gets digitized. An FPGA (Field Programmable Gate Array) processes the streams of multiple ADCs and transmits them for further processing. The cascaded amplifier design dissipates the power, needed for amplification, further away from the detector. The cooled detector is then able to measure electron events at an optimum resolution. Figure 4.1 shows the full signal chain, from the detector front-end to the first FPGA.

## 4.2. The JFET-Amplifier

The first amplification stage is a n-JFET which is integrated on the SDD. The charge from the detector gathers on the detector anode, and is buffered by the JFET in source follower configuration. The signal is coupled to the first amplifier, which has a feedback capacitance to the JFET gate. This style of feedback architecture – called 'charge sensitive amplifier' – allows to achieve higher bandwidths, than with a circuit that directly amplifies the voltage at the source of the JFET [22]. The schematic is shown in figure 4.2.

## 4.3. ETTORE Amplifier

A coarse internal schematic of the amplifier is shown in figure 4.2. The ETTORE amplifier has twelve channels, with two amplification stages. A DC coupled stage, outputting the ramp signals with the events, and an AC coupled stage, which outputs pulses with exponentially decaying tails. The RC time constant of the exponentially decaying tail is 15 $\mu$S, and is determined by the resistor R4 and capacitor C3. In order to keep the second stage output steady during the RESET pulse, the ETTORE receives a digital 0 - 3.3V inhibit signal, which short circuits the feedback capacitance of the second

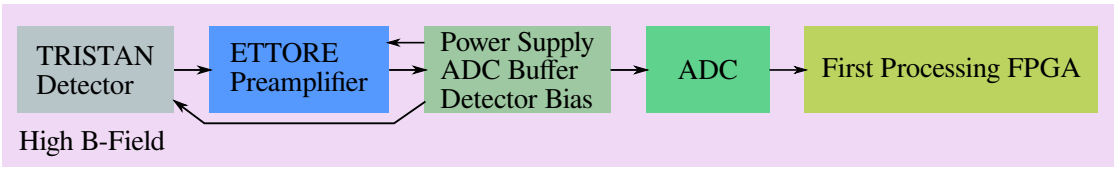



**Figure 4.1.:** Schematic image of the signal chain to the first processing stage. All of the electronics are in a high magnetic field environment of several Tesla.

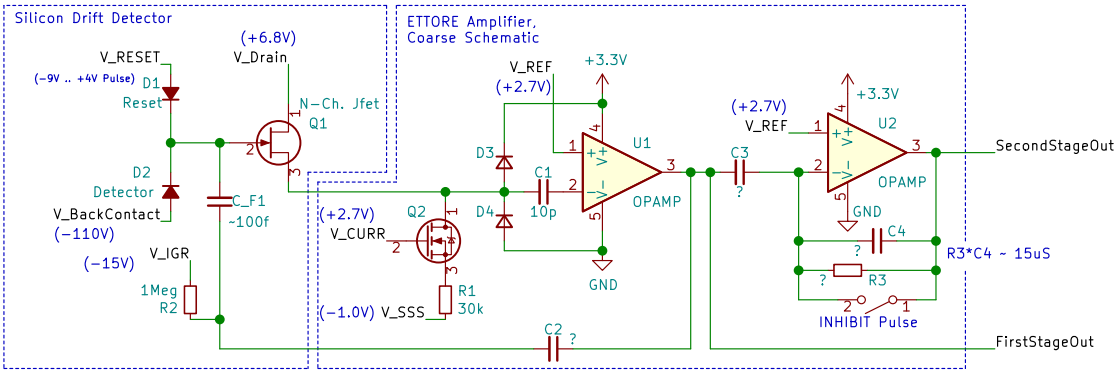



**Figure 4.2.:** Schematic depicting the detector front-end. Blocks surrounded by blue dashes lines are the detector with the integrated JFET, and the preamplifier ASIC called 'ETTORE'. It shows optimal operating voltages for the detector in blue brackets, and the labels show the commonly used names in the setup. Question marks show unknown values, as the ETTORE amplifier is designed by an external company [30].

amplifier, and brings the output to VREF. One ETTORE channel has only one output, so we can choose the desired signal with an analog multiplexer.

## 4.4. Buffer Amplifier

A buffer amplifier is needed in order to properly drive the analog to digital converter. The ETTORE amplifier provides a maximum current of a few milli-amperes, which is not sufficient to properly drive a high resolution, high speed ADC. Therefore another, more powerful signal buffer is needed. The buffer designed in this thesis has a gain of 2 and a bandwidth of 35MHz.

### 4.4.1. Buffer Gain considerations

The ETTORE supports two gain settings. An incoming electron with an energy of 1 keV produces an output step of 8.8 mV with the 'low gain' setting or 17.6 mV with the 'high gain' setting. This gain is selectable with a digital logic pin. In the KATRIN setup, depending on post-acceleration of the electrons of up to 20 keV, events with an energy close to 40 keV are expected. This means than one electron event, with the 'low gain' setting in the ETTORE, will produce a voltage step of $\approx 350$ mV. The ETTORE has an output dynamic range of 2V. With an event rate of $10^5$ electrons per second at the detector, the expectation value for time it takes for 5 events to a arrive at the detector is 50 $\mu$S. With a reset and inhibit pulse duration of approximately 2 $\mu$S, this would mean an approximate dead time of 4% due to resets.

## 4.5. Analog to Digital Converter

The analog to digital converter (ADC) is an electronic device, that transforms an analog signal into a stream of digital numbers. Further details about the ADC will be described in the chapter 7. Currently all prototype measurements are performed with ready to buy **d**ata **acq**uisition systems (DAQ) , either from the company Brucker XGLAB, or from CAEN Systems.

### 4.5.1. Resolution Estimation of the ADC

The resolution of the ADC should have 14 - 16 bits, in order not to be limited by quantization errors of the ADC. It's of interest to find a minimum viable resolution, as with that the cost of the ADC, and the complexity in operation goes down. As noise powers add up, the voltage amplitude is added geometrically, assuming the noise sources are uncorrelated. This is of interest when comparing ADC quantization noise to the detector signal noise. It's of interest to find an operating point, where the detector signal noise dominates and we can still use a low resolution ADC, without loosing signal resolution. It should be enough if the quantization noise amplitude is a quarter of detector signal noise amplitude, as this would increase the noise level from '1' to $\sqrt{1^2 + 0.25^2} = 1.03$. Figure 4.3 shows the noise level of a well shielded measurement of a 7 pixel prototype detector. The standard deviation of the noise amplitude is 14 LSB with a 16 bit ADC that operates at at input range from 0 - 3.3V. With a 14 bit ADC the standard deviation would be 3.5 LSB. With a quantization noise of 1/2 LSB, the quantization noise is 14% of the detector noise. When using a 14 bit ADC in comparison to a 16 bit ADC, the noise would only increase by 0.9% in amplitude.

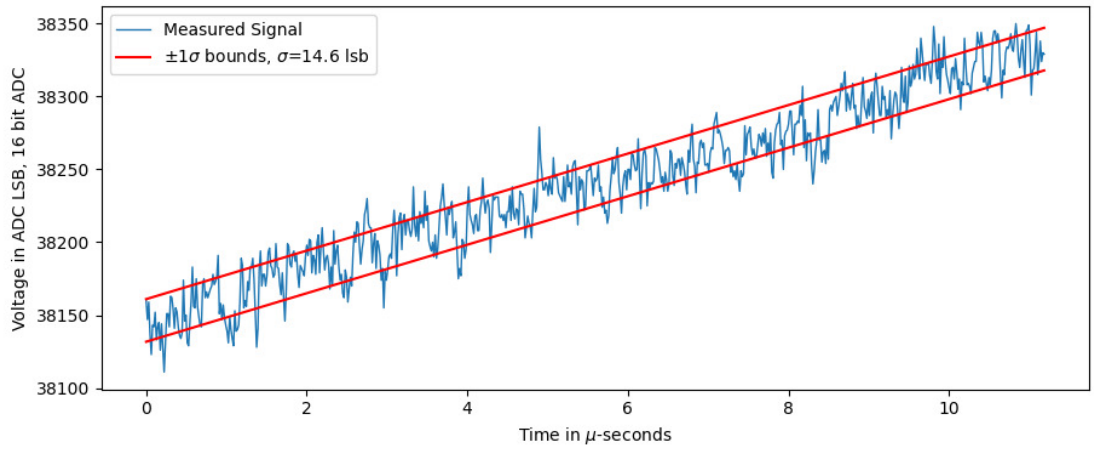



**Figure 4.3.:** The image shows the noisy signal ramp in blue, and the red lines show the boundaries of the standard deviation of this signal. The standard deviation of this signal is 14lsb for a 16 bit ADC, or 0.65mV

## 4.6. FPGA

The field programmable gate array (FPGA) processes the digital stream of the ADC filters the stream for particle events, optionally computes their energy and sends the data down to a further compute instance, most probably comprised of a crate with multiple FPGA's inside. FPGAs have advantageous parallelization capabilities, supporting multiple ADC channel readouts at once, with only one piece of silicon. Furthermore FPGAs can be reprogrammed, enabling quick development and test iterations. Regarding the TRISTAN design, the choices for the final FPGA and compute instances are yet to be made.

## 4.7. Rise Time and Buffer Bandwidth Considerations

The rise time of an event step can be used to classify the multiplicity of events, and otherwise not detectable energy loss at the border of the pixels. Furthermore, it's of interest to preserve the detector signal as well as possible, and necessary to analyze the signal chain with respect to the component rise times. For the following considerations, only the fastest signal rise times are of importance, as a fast signal chain is also able to support slower signals.
The bandwidth limiting component in the signal chain should be the detector, and all following components should only have a minor influence on the rise time.

### 4.7.1. Rise Time Theory

Every analog electronic stage has it's intrinsic maximum bandwidth $f_{BW}$, at which it can still process a signal. With an increasing input frequency above $f_{BW}$, the output signal amplitude of the electronic stage drops, until no output is visible at all. Usually $f_{BW}$ is determined by the point where the output signal drops to 70% of it's nominal value. This is commonly called the -3dB point.
This maximum bandwidth $f_{BW}$ is directly related to the fastest rise time this electronic stage can support:

$$t_{rise} \approx 0.34/f_{BW} \tag{4.1}$$

This result can be either calculated by assuming a gaussian frequency response $H(f) = e^{\frac{-\omega^2}{\sigma^2}}$, and applying the step response to the Fourier transform $\mathcal{F}(H)$, and finding the time it takes for the signal to rise from 10% to 90%, or a numerically very similar value, by analyzing the time response of an RC low pass filter, with the time constant $\tau = RC = \frac{1}{2\pi f_{BW}}$.
Now assume an experiment, where you feed an infinitely sharp signal step into two cascaded amplifier stages, as shown in figure 4.4. Each stage has it's associated $f_{BW}$, and risetime $t_{rise}$. The combined rise time of this system is the geometric mean of the rise times.

$$t_{rise,combined} = \sqrt{t_{rise,1}^2 + t_{rise,2}^2} \tag{4.2}$$

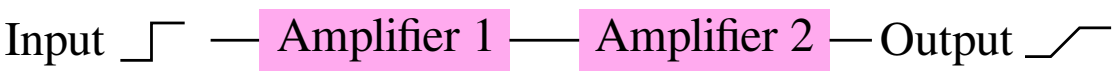



**Figure 4.4.:** Two cascades amplifiers, with an input signal, that is an infinitely sharp step. The output signal rise time depends on the geometric mean of the rise times of each of the amplifiers

### 4.7.2. Determining the ADC Sampling Frequency for our Signal Chain

Finding an adequate ADC sampling frequency is of significance, as a too slow ADC would distort the signal and loose information, and a too fast ADC would generate more heat on the PCB, cost more, and generate useless data which in turn would have to be transmitted to the main compute instance, requiring unnecessary transmission channels and compute power.
Rise time and bandwidth measurements of several components were made, based on which I calculated other unmeasured component values. The measurement setups and results are listed in table 4.7.2:

| Measured Component / Signal Chain | Result and Note |
|---|---|
| XGLAB bufferboard | $f_{BW} = 20.1\,\text{MHz}$<br>measured with Vector Network Analyzer |
| Bufferboard<br>by Jakov Kholodkov (thesis author) | $f_{BW} = 35\,\text{MHz}$<br>measured with Vector Network Analyzer<br>result in figure 5.14<br>on page 31 |
| DANTE DAQ | $f_{sample} = 62.5\,\text{MHz}$<br>$t_{rise} = 16\,\text{nS}$<br>[14] |
| Agilent 81110A 2nS Generator →<br>ETTORE 1st Stage →<br>Rhode&Schwartz RT Oscilloscope<br>at $f_{BW} = 500\,\text{MHz} \rightarrow t_{rise}$ | Measured risetime:<br>$t_{rise} = 12.2\,\text{nS}$<br>[11] |
| Agilent 81110A 2nS Generator →<br>ETTORE 1st Stage →<br>ETTORE 2nd Stage →<br>Rhode&Schwartz RT Oscilloscope at<br>$f_{BW} = 500\,\text{MHz} \rightarrow t_{rise}$ | Measured risetime:<br>$t_{rise} = 16.8\,\text{nS}$<br>[11] |
| Detector with $^{55}$Fe Events →<br>ETTORE 1st Stage →<br>XGLAB bufferboard →<br>DANTE DAQ → $t_{rise}$ | Shortest risetime in distribution:<br>$t_{rise} = 30\,\text{nS}$<br>[14] |

Using the listed measurement results, and equations 4.1 and 4.2, I calculated the internal rise times and the bandwidths of the components, which are listed in table 4.7.2. The reason, why for most values the uncertainties are omitted, is that they have been measured with precision devices, and are for experimental purposes negligibly small. The value for the detector risetimes has been calculated using the distribution from [14][p.45], and read off of the chart using the computer program Inkscape, reading a value of $32.5 \pm 1$ nS. These detector risetimes are from real x-ray events from a $^{55}$Fe source.

| Component | Ristime $t_{rise}$ | Bandwidth $f_{BW}$ |
|---|---|---|
| Fastest Risetime from Detector: | $19.1 + 1.7$ nS | 16.2 .. 18.3 MHz |
| ETTORE 1st Stage $t_{\text{rise}}$: | 12.0 nS | 29.1 MHz |
| ETTORE 2nd Stage $t_{\text{rise}}$: | 11.6 nS | 30.3 MHz |
| XGLAB 48 Channel Buffer: | 17.1 nS | 20.5 MHz |
| Jakov 48 Channel Buffer: | 10.3 nS | 35.0 MHz |

When deciding for an ADC, it's best to support the fastest combination of components: Using the fastest rise time of the detector, only the first stage of ETTORE, and the faster buffer. Inserting the values into eq. 4.2 yields:

$$t_{\text{rise,combined}} = \sqrt{t^2_{\text{rise,detector}} + t^2_{\text{rise,ETTORE 1st Stage}} + t^2_{\text{rise,JakovBuffer}}} = 24.67\,\text{nS} = \quad (4.3)$$

This value sets a lowest boundary for the sampling interval of the ADC, requiring a sampling frequency of:

$$f_{\text{ADC,sample}} = \frac{1}{t_{\text{rise,combined}}} = 40.5\,\text{MHz}$$

When using the XGLAB buffer with a bandwidth $f_{BW} = 20.5\,\mathrm{MHz}$ the final fastest rise time would be 28.2 nS, and would require an ADC with $f_{\mathrm{ADC,sample}} = 35.3\,\mathrm{MHz}$.

## 4.8. Digital Signal Processing and Event Energy Measurement

The algorithm, which processes the step-like signal consists of two filters, one filter for triggering and one for energy measurement. Applying a filter $F(t)$ to a signal $\mathcal{S}_{\mathrm{in}}(t)$ is the convolution of the filter function with the signal.

$$\mathcal{S}_{\mathrm{out}}(t) = \int_0^T \mathcal{S}_{\mathrm{in}}(t-\tau) \cdot F(\tau) d\tau$$

The filter function $F(t)$ is assumed zero outside the time interval $[0 : T]$. The DANTE DAQ, uses two trapezoidal filters, one for event triggering and one for energy measurement. The filter response function is shown in figure 4.5. The peaking time region $t_{\mathrm{peak}}$ is for averaging the signal before and after the step. For the duration of the flattop time $t_{\mathrm{flattop}}$ the signal is ignored, which accounts for the rise time of the signal. The reason this filter is called a trapezoidal filter, is the shape of the output signal, after

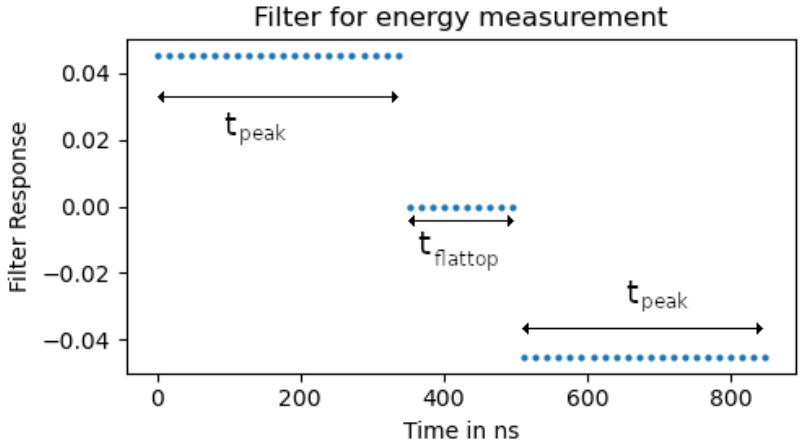



**Figure 4.5.:** The impulse response of the trapezoidal filter, with peaking time $t_{\mathrm{peak}}$ and flattop time $t_{\mathrm{flattop}}$.

the convolution. When the trigger filter shoots above a certain threshold, the energy measurement of the second filter is evaluated. The height of the energy trapezoid is proportional to the step-height, as shown in Figure 4.6. With two parallel filters, we achieve a much better pile-up rejection than with one. Furthermore, when modifying the trigger filter to a 'fast triangle' filter, pile up rejection can be even further improved [32].. For further reading, Martin Descher [12] analyzed the properties of the trapezoidal filter in great detail [p. 44 - 68]. Especially of interest is the formulation of the filter as a recursive, infinite impulse response (IIR) filter, as it dramatically reduces computation time, compared to using a convolution.

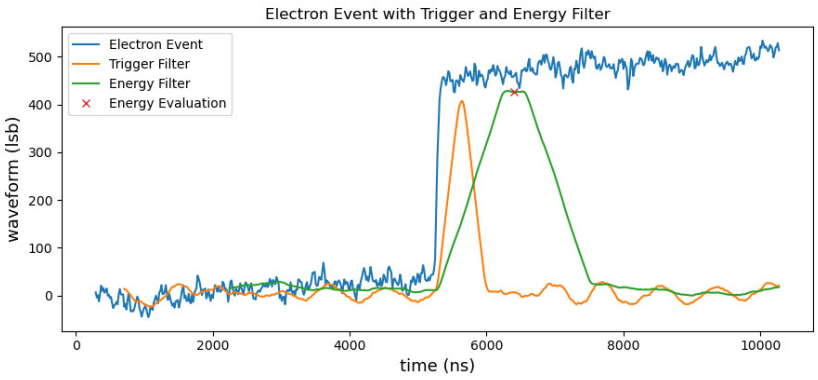



**Figure 4.6.:** An electron event, and the signals after a fast trigger filter and a slower energy filter have been applied. The Energy is evaluated at the center of the slow trapezoidal filter.

# Chapter 5.

# Bias Board

The design and development of the TRISTAN bias board was the main work of this master thesis. I describe where the bias board is located in the KATRIN project, and what functionalities it has to fulfill. The final TRISTAN detector, each 166 pixel detector tile will be operated by it's own 'tile main board'. All the developed circuits will be located on the tile main board. Figure 5.1 shows a block diagram of the setup. The light blue blocks were the topic of this thesis. To test those blocks, they were build on separate circuit boards. This chapter explains those schematics, and then shows their real world performance. The two blocks are:
The bias board which supplies the voltages for the detector and the ETTORE preamplifier, and a high speed buffer amplifier, which properly drives the ADC inputs.

**General Requirements** All of the electronics will be located in a magnetic field on the order of 1 Tesla. This poses a challenge for electronics with inductors. For commercially available inductor core materials the saturation magnetic field $B_{sat}$ ranges from 0.5 – 1.8 T. Above this magnetic field, the magnetic permeability of the core and therefore the inductance decreases - changing the electric properties of the circuit. Only air-coils can be used safely, as the magnetic flux density has no noteworthy effect on the magnetic permeability of air. If inductors are not strictly required, it's recommended to completely exclude them from the design.
The table 5.1 shows the required voltage ranges to operate the detector. It was taken as a guideline for the whole design.

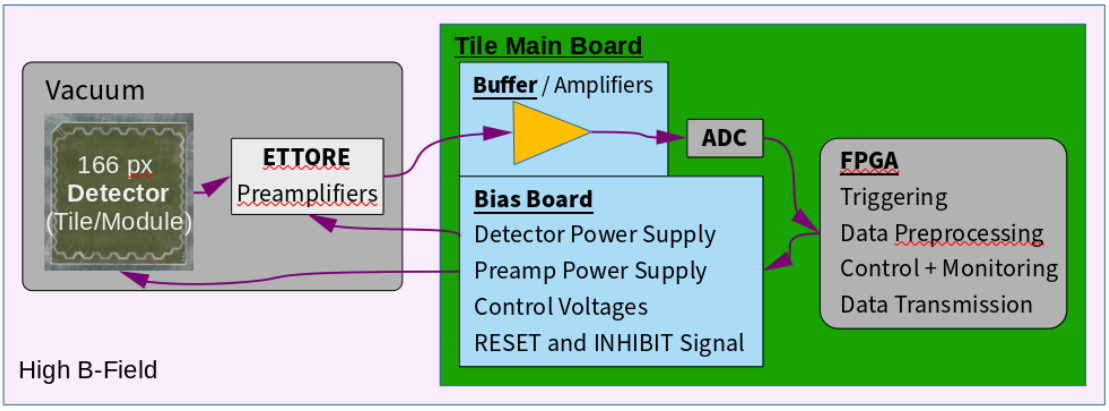



**Figure 5.1.:** A block diagram of the planned electronics setup for the final TRISTAN detector. Blocks in light blue indicate the circuits that I have been working on.

| Name | Description | Set-point | Operation Range | Set-point Current | Max Current | Voltage Monitoring | Current Monitoring |
|---|---|---|---|---|---|---|---|
| $V_{BC}$ | Back Contact | -100 V | -80 V to -120 V | $<$ 10 nA | 100 nA | (X) | |
| $V_{BF}$ | Back Frame | -110 V | -90 V to -130 V | $<$ 10 nA | 100 nA | (X) | |
| $V_{R1}$ | Innermost Bias Ring | -8 V | -5 V to -15 V | -3 mA | -5 mA | (X) | |
| $V_{RX}$ | Outermost Ring | -120 V | -100 V to -150 V | 3 mA | 5 mA | (X) | (X) |
| $V_{IGR}$ | Inner Guard Ring | -15 V | -15 V to -35 V | $<$ 10 uA | nA | (X) | |
| $V_{D}$ | JFET Drain Voltage | 7 V | 5 V to 10 V | 17 mA | 60 mA | (X) | (X) |
| $V_{SSS}$ | Current Source | -1 V | -20 V to 2 V | 17 mA | 60 mA | (X) | (X) |
| $V_{ASIC3V9}$ | ETTORE Supply | 3.9 V | fixed | 840 mA | 1200 mA | | |
| $V_{CURR}$ | Current Source Gate | 2.7 V | 1.0 V to 3.3 V | $\sim$ 20k$\Omega$ to 2.7V | | | |
| $V_{REF}$ | ETTORE reference | 2.7 V | 2.0 V to 3.0 V | $\sim$ 20k$\Omega$ to 2.7V | | | |
| $V_{TH}$ | Threshold For Reset | 2.7 V | 1.0 V to 3.0 V | $\sim$ 20k$\Omega$ to 2.7V | | | |
| $V_{BW}$ | Bandwidth Compensation | 1.0 V | 1.0 V to 3.0 V | $\sim$ 14k$\Omega$ to 1.0V | | | |
| LG | enable low gain mode | 0 V | CMOS Digital | | | | |
| SELECT_PRE | enable first stage output | 0 V | CMOS Digital | | | | |
| INH | inhibit ETTORE | 0 V | CMOS Digital | | | | |
| RESET | Detector Diode Reset | -10 .. +4V | Short Pulse | peak current $\sim$ mA | | | |

**Table 5.1.:** Requirements table for the Design of the Bias System

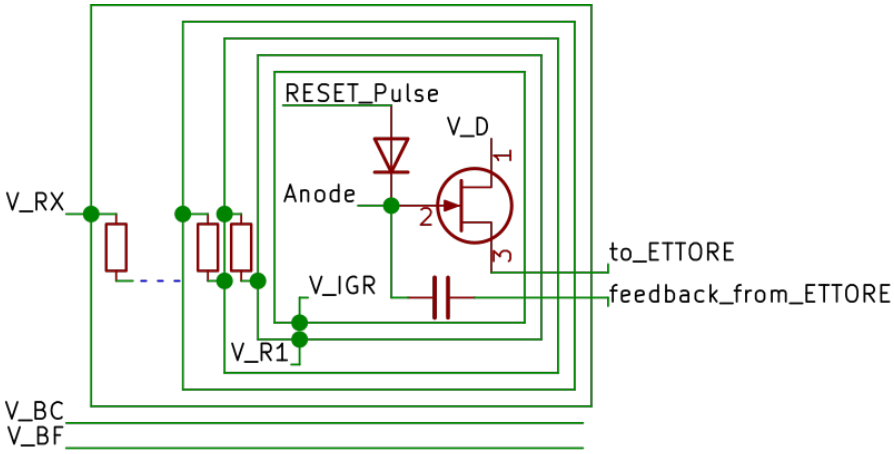



**Figure 5.2.:** A schematic indicating the voltages connected to the detector

**Detector Related High Voltages** Figure 5.2 shows the voltages which are connected to the detector. All the drift rings are connected with a resistor chain, so at each drift ring, there is a different potential, which guides the electron cloud within the detector to the anode. The innermost drift ring is called $\text{Ring}_1$, and the outermost $\text{Ring}_X$. The RESET signal is connected via a diode to the anode. This diode is reverse biased by default, and conducts current for the short time periods, to flush the accumulated charge from the anode. The integrated JFET works as a transimpedance amplifier, which then passes the detector signal to the ETTORE preamplifier. The voltages $V_{BC}$ and $V_{BF}$ are applied on the entrance window side of the detector and create a well defined drift-potential within the detector. The voltage $V_{IGR}$ is applied to a protective guard ring around the detector anode, to minimize noise.
All other voltages are indicated in figure 4.2 on page 12.

### 5.0.1. High Voltage Supplies

There are 5 high voltage supplies, that need to source little amounts of current at a voltage of up to 130V. There are 4 high voltage supplies that have to sink current, and Ring1 supply has to source current. The high voltage supply needs to be adjustable, in order to find an optimal setting for each detector tile, in terms of electron energy resolution. Ideally, the adjustment should happen digitally. The requirement to the absolute precision of the high voltages is relaxed, as it can be digitally calibrated, and it's enough, if the high voltage can be controlled in 200mV steps. Furthermore, the detector has an optimal operating region plateau of several volts on multiple voltages. Low drift and repeatability are of big importance. Furthermore the low ripple is important for a continuous, stable biasing of the detector.
For the adjustable high voltages, there are three options: charge pump circuits, transformer based converters and linear regulators. Transformer based converters are excluded due to the high magnetic field. The output of a charge pump ripples, and is therefore not suited for this use. The circuit of choice that's left is a linear regulator. It has all the desired requirements, with the drawback of dissipating power, in order to adjust for the right voltage. At the time of the design of this circuit, linear regulators for this high voltage were not readily available and were built discretely.
Half a year into the build process, after the first successful tests of the high voltage

supplies, Texas Instruments released the OPA462 operational amplifier which could probably do the same job with fewer components and less board space.

### 5.0.2. Working Principle of a Series Linear Regulator

Imagine having a detector with a resistance $R_D$ that needs a specified voltage of -120V, at a current of 1 mA, but the power supply only supplies -200V. The simplest way is to connect an 80 kΩ resistor $R_2$ in series, such that 80V drop across this resistor at a current of 1 mA. The resistor dissipates the excess energy, and -120V are supplied to the detector. A linear regulator works as a series resistor $R_2$, but it supplies 120V to the detector resistance $R_D$, independent of the current it is drawing. For that to work, it's necessary to continuously monitor the voltage across $R_D$ and continuously adjust the resistance of $R_2$.
The functioning blocks are shown in figure 5.3. It shows the resistor divider with the detector load, and a transistor which is adjusted such that the voltage drop across the detector is constantly 120V. The linear regulator designed in this thesis is adjustable

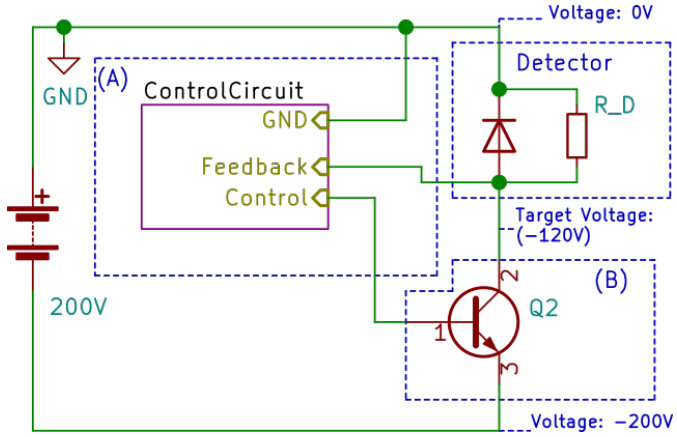



**Figure 5.3.:** The (A) section shows the control circuit which adjusts the transistor (Q2) in the (B) section, such that the voltage across the detector is 120V.

with a control voltage $U_C$, ranging from (0 .. +3.0V), proportionally outputting a high voltage of (0 .. -200V).

## 5.1. Sinking High Voltage Linear Regulator

The sinking linear regulator is required for four voltage supplies of $V_{BC}$, $V_{BF}$, $V_{RX}$ and $V_{IGR}$. In the following section I will introduce all sub-circuits and concepts, that make up the sinking linear regulator. For better understanding, I removed all protection circuitry from the schematic. A simplified schematic of the high voltage linear regulator is shown in 5.4. The full schematic with protection circuitry is shown on page 26, in figure 5.8. The blue boxing is drawn for direct comparison, in order to see the coarse functionalities of the blocks, when comparing to figure 5.3.

**Working Principle** The regulator works on the principle, that the OpAmp keeps its negative input continuously at 0V. In order to achieve that, it drives the currents through (Q1) and (Q2), such that the currents through (R1) and (R2), $I_{R1}$ and $I_{R2}$ are equally big $I_{R1} = -I_{R2}$. With Ohms Law directly follows the relation between control voltage

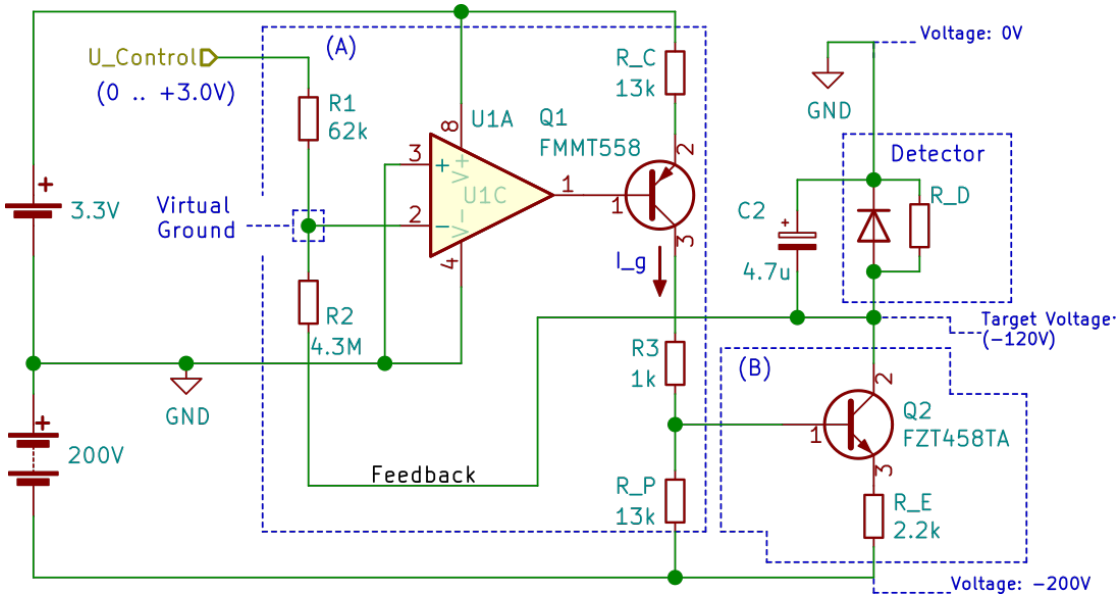



**Figure 5.4.:** Linear regulator schematic without protection circuitry.

$U_C$ and output voltage $U_O$:

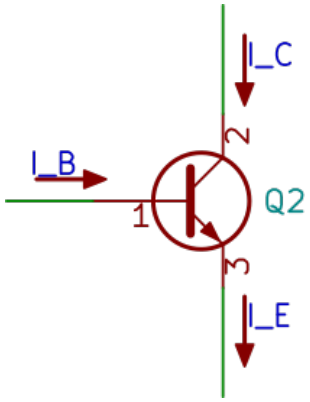
$$\frac{U_C}{R_1} = \frac{U_O}{R_2} \tag{5.1}$$

When evaluating this schematic as an amplifier with signal input $U_C$ and signal output $U_O$ the gain is $G = \frac{R_1}{R_2} = \frac{4.3e6}{62e3} = 69.3 \approx 70$.

### 5.1.1. Current Limiting of the Linear Regulator

Current limiting is a safety guard required by any electronic device, to protect against damages of too high current draw, especially, when working with high voltages. With linear regulators, there are two kinds of current limiting architectures:
The 'constant current limit' does not allow more current to flow, than specified. The 'foldback current limit' actively reduces current flow, once a specified limit is hit. I chose the 'constant current limit' for this regulator, as it is simpler to build. The foldback current limiting can be implemented in software, as the output voltages are monitored and would drop well below the set-point. This can be used to lower the control voltage to a minimum.
For biasing the drift rings within the detector one of the supplies needs to have a current limit of 6 - 7mA. In a worst case short circuit, the maximum dissipated power is 1.3W, for the time it takes for the software to react, and intervene. Short circuits occurring after the linear regulator, might damage sensitive electronics, but are very improbable to cause fire or a damaging amount of heat dissipation. In order to calculate the maximum current in this schematic, it's necessary to inspect, what limits the current through the NPN transistor (Q2): The NPN transistor (Q2) has a current gain $\beta \approx 120$ which determines by how much the base current $I_B$ is amplified as collector current $I_C$: Both currents $I_C$ and $I_B$ add up to the emitter current $I_E = I_B + I_C$. With high current gain transistors, it's common to approximate $\beta \approx \beta + 1$, and therefore approximate $I_E \approx I_C$. Using Kirchhoffs laws one arrives at the base current through the transistor (Q2):

$$I_B = \frac{I_g \cdot R_P - 0.6}{\beta \cdot R_E + R_P} \tag{5.2}$$




**(a)** Nomenclature of NPN Transistor currents

$$I_C = I_B \cdot \beta$$
$$I_E = I_B + I_C = I_B(1 + \beta)$$

**(b)** Equations of the NPN transistor

The only unknown is the current $I_g$: The operational amplifier (OpAmp) controls the current $I_g$ through the PNP transistor (Q1) figure 5.4. The maximum value of $I_g$ is

$$I_g = \frac{2.7V}{\mathrm{R}_C} = \frac{2.7V}{13k\Omega} \approx 200\mu A, \tag{5.3}$$

as the PNP transistor ((Q1) figure 5.4) is in an emitter follower configuration, and the potential at (Q1: pin 2): $U_{(\mathrm{Q1:Pin2})} = U_{(\mathrm{Q1:Pin1})} + 0.6V$, so the maximum voltage drop across the resistor $\mathrm{R}_C$ is $3.3V - 0.6 = 2.7$. The resistor $R_3$ is for protective measures - and does not play a noteworthy role in limiting the load current. Plugging in the values and combining equations 5.8 and 5.2 one arrives at the maximum collector current:

$$I_{C,max} = \frac{\beta \cdot (I_g \cdot R_P - 0.6V)}{\beta \cdot R_E + R_P} = \frac{120 \cdot (2 \times 10^{-4}\,\mathrm{A} \cdot 13 \times 10^3\,\Omega - 0.6\,\mathrm{V})}{120 \cdot 2.2 \times 10^3\,\Omega \cdot 13 \times 10^3\,\Omega} \approx 870\,\mu\mathrm{A} \tag{5.4}$$

In transistor production $\beta$ is a strongly fluctuating factor, changing from waver to waver. In order to reducing the influence of $\beta$ fluctuations, $R_P$ works as a degeneration resistor.

### 5.1.2. Current Monitoring

It's required to measure the current that flows into the $\mathrm{Ring}_X$ pin. Current measurement commonly works using either a hall sensor, or a shunt resistor. For the case of a few mA of current, a shunt resistor is a viable option. The small voltage drop across the shunt resistor must be amplified, and directed to a supervisor ADC, for example in a micro-controller. The current is measured at a high potential, and the information must be brought to a lower potential. The working principle of this circuit is adapted from [29][p.84; and LTC6101]. The following text references the schematic in figure 5.6. For the power supply of the OpAmp (U2), the shunt amplifier, I use a constant current source supplying 1mA. The zener diode (D1) makes sure that the OpAmp (U2) is supplied with 8.2V. The OpAmp (U2) must have a very high input impedance, in order to not distort the measurement across the shunt resistor. A fitting OpAmp is the LMP7701, as it has the additional benefit of only consuming 715 $\mu$A of current, and therefore operating with a low power dissipation at the supplying constant current source and diode (D1). The current flowing through the shunt resistor $R_{\mathrm{Shunt}}$ creates a voltage drop. The OpAmp (U2) makes the current $I_R$ pass through the transistor (Q2), such that the potentials at its positive and the negative inputs are equal, which leads to:

$$I_S \cdot R_{\mathrm{Shunt}} = I_R \cdot R_4 \tag{5.5}$$

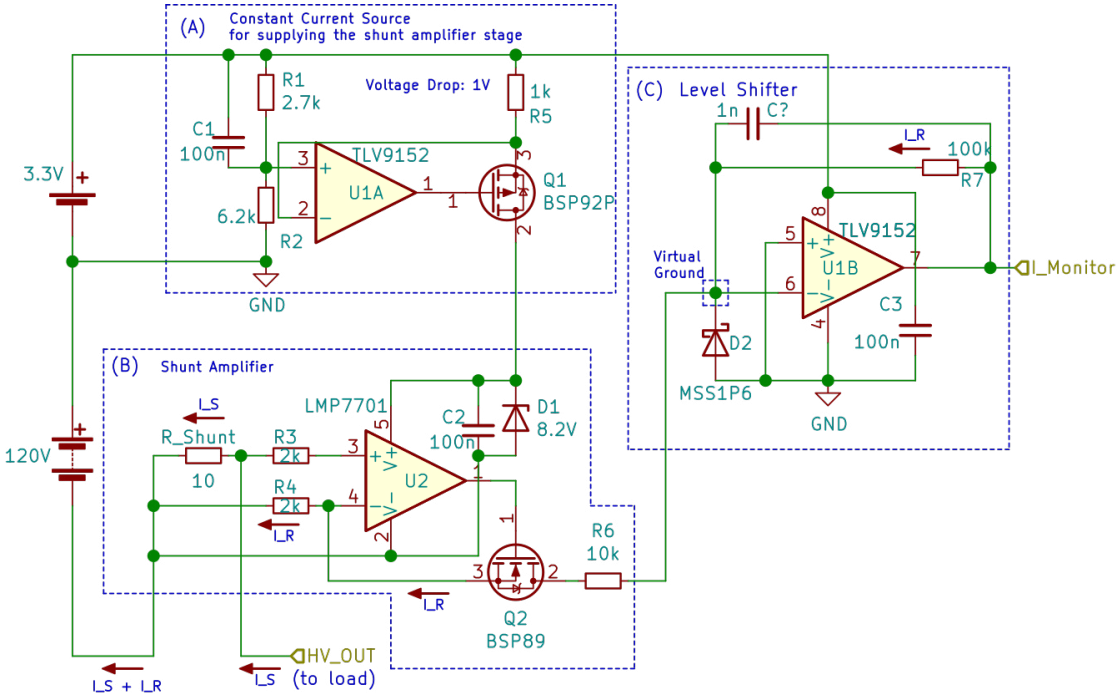



**Figure 5.6.:** Circuitry of the Current Monitor. (A) Shows the constant current supply of 1mA, going to (B), the shunt resistor amplifier. In combination with the transistor (Q2) section (C) shifts the voltage into a range from (0V .. 3.3V).

The only source of the current $I_R$ is the output of the OpAmp (U1B), which flows through the resistor (R7). Again, the OpAmp (U1B) needs to have a very low input bias current, in order not to disturb the measurement. The output potential of OpAmp (U1B) at the label "I_Monitor" is called $U_{\text{mon}}$. With

$$I_R = \frac{U_{\text{mon}}}{R_7} \tag{5.6}$$

and equation 5.5 follows

$$U_{\text{mon}} = I_S \cdot R_{\text{Shunt}} \cdot \frac{R_7}{R_4} \tag{5.7}$$

So the gain of the amplifier with the level shifting stage is determined by

$$G = \frac{U_{\text{mon}}}{I_S \cdot R_{\text{Shunt}}} = \frac{R_7}{R_4}$$

, with $G = 50$ in our case. With this given configuration it's possible to measure currents up to 6.6 mA.

**Non-linearities of the Input Voltage and Drift effects** Here I estimate the worst case distortions, which could happen during current measurement. The gate leakage of the transistor (Q2), the input bias currents of both (U2) and (U1B) cause a minor distortion to the measurement. The gate leakage currents in all involved transistors are in the range $I_L < 10nA$, so the additional voltage drop caused by the sum of those leakage currents, would cause at maximum distortion in measurement result of $3 \cdot I_L \cdot G < 2.1\mu A$, which is at worst $\sim 1/3000$ of the whole measurement range. This corresponds approximately to 1.33 LSB (least significant bit) for a 12 bit ADC - which is very little. Thermal

effects, which change the amplifier input offset voltage, play a slightly bigger role during operation. The OpAmp LMP7701 has a specified input voltage offset drift of $1^{\mu V}/_{\circ C}$, and $5^{\mu V}/_{\circ C}$ at temperature extremes. approximating an average of $2^{\mu V}/_{\circ C}$ of input offset voltage drift, this would correspond to a current measurement error of $I_{err} = 12\mu A$ for a temperature jump of 60 °C. This is acceptable for monitoring proper operation of the detector.

$$I_{err} = \frac{U_{err}}{R_{\text{Shunt}}} = \frac{2^{\mu V}/_{\circ C} * 60°C}{10\Omega} = 12\mu A$$

### 5.1.3. High Voltage Monitoring

The high voltage monitoring circuit is a simple inverting amplifier, with a gain $G = 1.44 \cdot 10^{-2}$. The circuit is shown in figure 5.7.

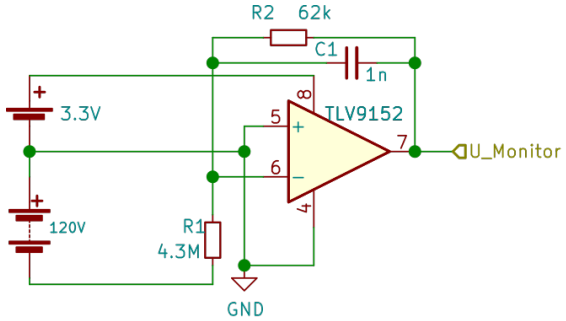



**Figure 5.7.:** Circuitry of the voltage monitor as a simple inverter, with gain lower than 1. The 120V battery supplies the voltage to be monitored.

### 5.1.4. Full Schematic of the Series Linear Regulator with monitoring

After combining the linear regulator, the voltage and the current monitor, one arrives at the circuit in figure 5.8.

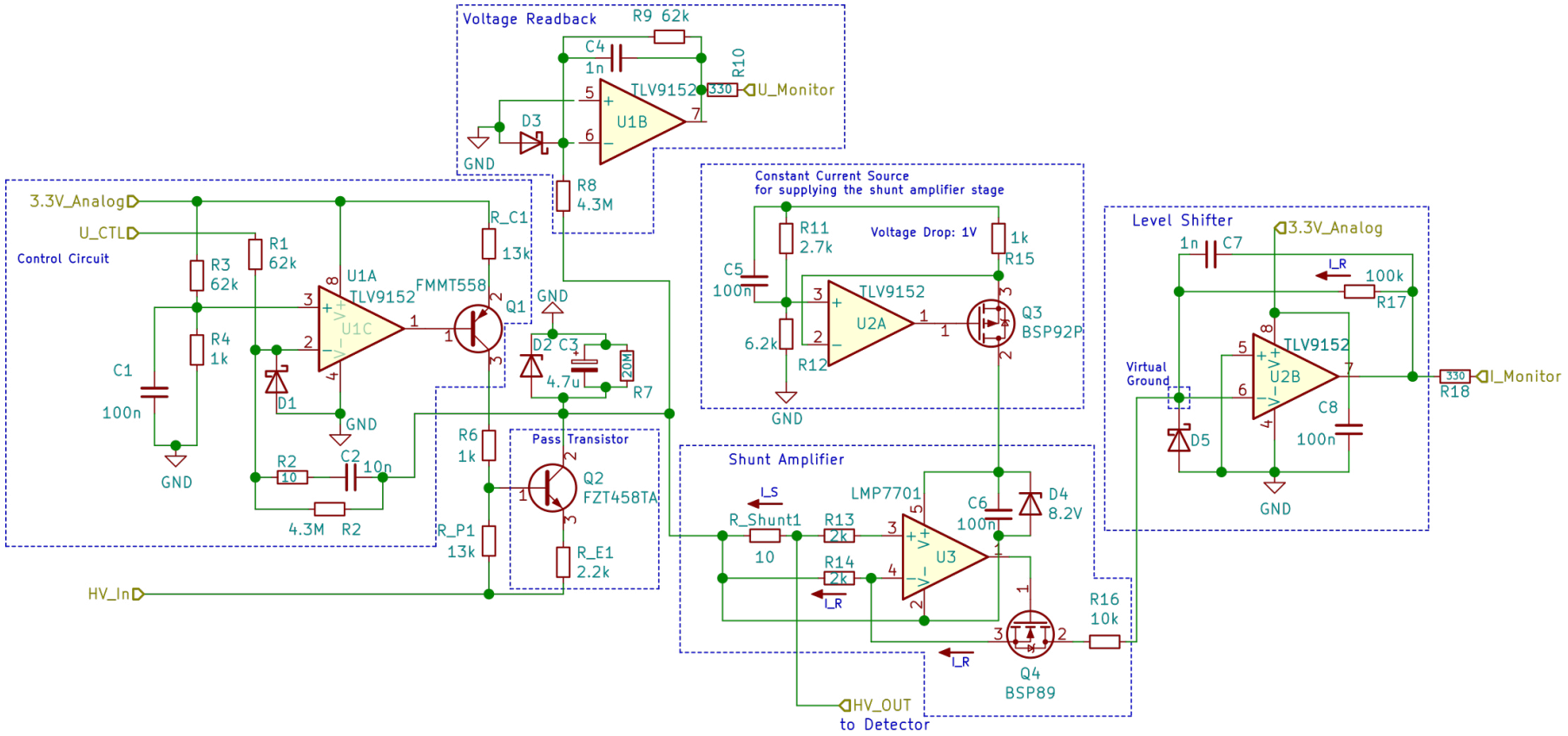



**Figure 5.8.:** Schematic of a full regulator with current and voltage monitoring.

**Operational Amplifier Input Offset Voltage, and Correct Startup Behaviour** The linear regulator must never output an uncontrolled voltage at it's output, independent of the order, at which the low and high voltage supplies are applied. This behavior can be undermined through the OpAmp input offset voltage. The input offset voltage is an effect arising from nonidentical input transistors of the OpAmp. An ideal OpAmp output goes to ground, when both input are connected together to the same potential. On contrary, a real OpAmp needs a very small potential difference between it's inputs – the input offset voltage – in order for the output to ground. At startup, when the control voltage is at the ground potential, the input offset voltage could cause the same effect as a small control voltage - and cause unpredictable voltages at the output. In order to control this, it's necessary to set the positive input at a small, definite potential $U_{\text{Offset}}$; so in default mode, the OpAmp outputs the positive supply voltage, blocking any current from flowing through the PNP transistor. The voltage $U_{\text{Offset}}$, is delivered by two resistors R3 and R4 in Figure 5.8. This causes a small shift in the output voltage, shown in equation 5.8.

$$U_O = (U_C - U_{\text{Offset}} + U_{\text{OpAmpInputOffset}}) * \frac{R_2}{R_1} \tag{5.8}$$

**Protection Circuits in the Full Schematic** It's necessary to protect operators, who work with the circuits from dangerous high voltages. Capacitors of 4.7$\mu$F store approximately 1/10 of a Joule at 200V, with $E = 1/2 CU^2$. This is not enough to injure a healthy person, but enough for a hurtful zap, and it might damage sensitive electronics when the operator touches sensitive lines, while accidentally touching the capacitor. In order to avoid that, the bleeding resistor (R7) with 20 M$\Omega$ is installed in parallel to the output capacitor. This bleeding resistor makes sure that after the time of approximately 2 minutes, the voltage at the capacitor has reached a safe operation level of 48V. The inputs of the OpAmps are sensitive to voltages that go beyond the supply rails, so Schottky diodes (D1),(D2),(D3) and (D5) protect the voltages from going 0.2V below ground.

### 5.1.5. Stability of the Linear Regulator

The stability of the regulator is very important, in order to preserve the measurement quality. A measurement of the output voltage is shown in figure 5.9. It shows a noisy signal with an amplitude of $V_{PP} \approx 1\,\text{mV}$. This agrees well with simulation, as compared to figure A.2 on page 29. The key to such a measurement is a fully coaxial cabling, with minimal wire-loops. The long term stability of the linear regulator is compromised, as shown by long term measurements in figure 5.10. I measured the effect later during my thesis and haven't invested the time in fixing it. The reason for this instability is a dependence of the output voltage on the ambient temperature around the regulator. The thermally sensitive element in the schematic is the resistor ratio of $\frac{R_2}{R_1} = G$ from schematic 5.8, which is responsible for setting the gain of the linear regulator is also temperature dependent. When estimating a worst case temperature coefficient of the resistor divider, of $R_1$ at $+100^{\text{ppm}}/^{\circ}C$ and of $R_2$ at $-100^{\text{ppm}}/^{\circ}C$ , the gain error amounts to $\frac{\mathrm{d}G}{\mathrm{d}T} = G \cdot 200^{ppm}/^{\circ}C$. With a temperature fluctuation of 8 °C this amounts to a voltage fluctuation of 80 mV. This value has the correct order of magnitude. The influence of the OpAmp (U1A) is minimal to the temperature dependence. This was an engineering mistake, caused by insufficient experience. This amount of random walk may be acceptable for

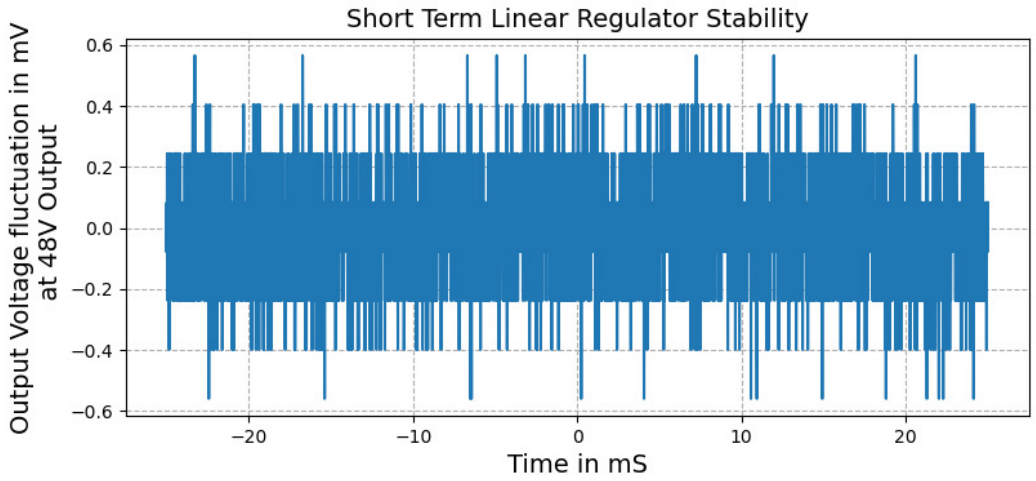



**Figure 5.9.:** Short term stability of a High voltage linear regulator, measured in mV. The resolution of the used oscilloscope is at the limit. The short term fluctuation is sufficiently low, to be used for measurements.

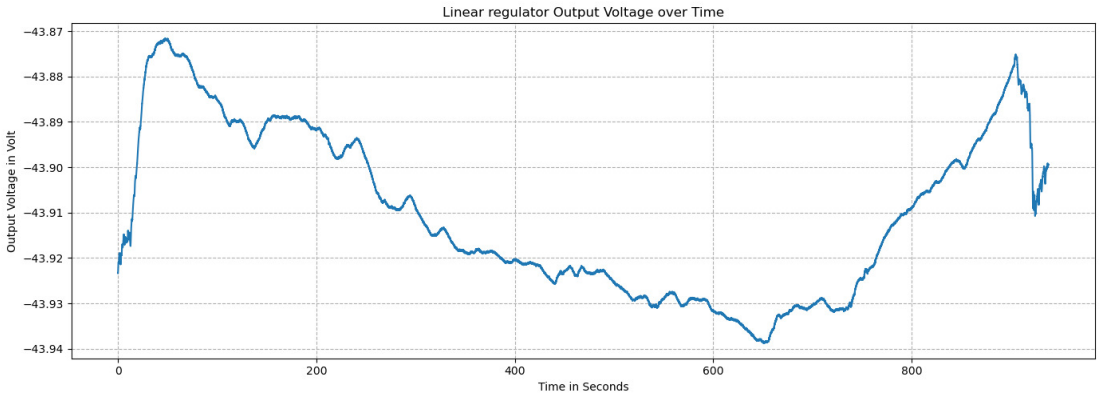



**Figure 5.10.:** Long term output voltage of the linear regulator. The visible amplitude are 70mV over the time of $\sim$ 16 minutes. The cause of the sharp rising edge in the beginning is me warming the schematic by blowing warm air over it. The cause of the sharp falling edge is me cooling the schematic by blowing ambient temperature air over it.

the detector operation, as the optimum operating voltages for the detector all have an accepted range, within which the resolution does not change. An improvement would be to use a resistor divider in one single package, which provides a ratio temperature dependence of $1 - 2^{ppm}/^{\circ}C$
Further component and schematic measurements are required to find the culprit with certainty.

## 5.2. Sourcing High Voltage Linear Regulator

The sourcing linear regulator supplies the voltage of the innermost drift-ring $R_1$ of the detector. The set-point of $R_1$ is 8V. The souring linear regulator, shown in figure 5.11 works on the same principle as the sinking linear regulator from the section above, but the main resistive element is not a NPN bipolar junction transistor, but a MOSFET (Metal Oxide Semiconductor Field Effect Transistor). The sourcing high voltage linear regulator does not need any current protection, as it sources it's current over the drift-

ring resistors into a sinking linear regulator, which has an overcurrent protection. The

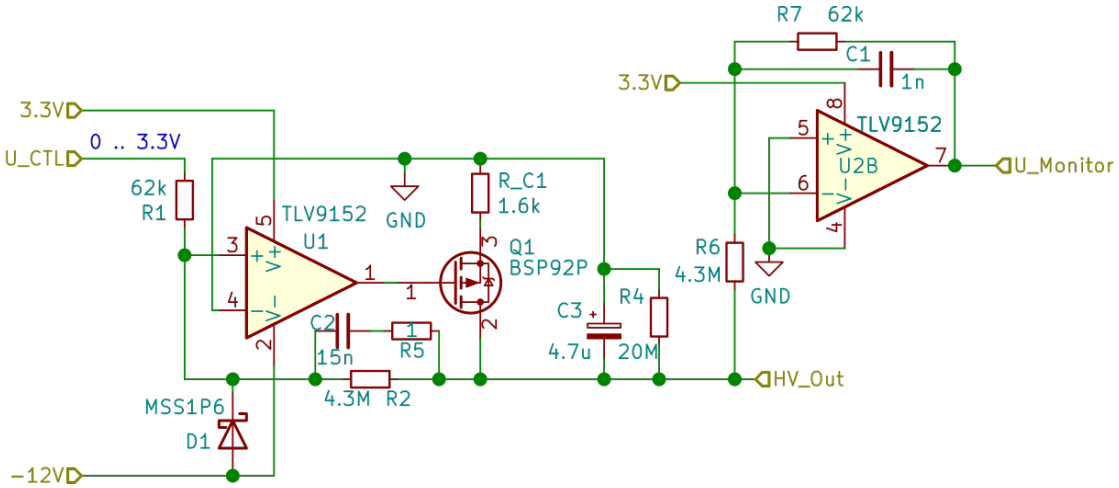



**Figure 5.11.:** The schematic of a sourcing linear regulator, with the MOSFET (Q1) being the main resistive element, that sources current from ground to a negative high voltage.

sourcing linear regulator suffers from the same long term stability problems as the sinking linear regulator. Further investigations are required.

## 5.3. Low Voltage Supplies

The low voltages supplies have the same requirements as the high voltages, regarding low noise, stability and repeatability, but should be controllable in smaller, 10 mV steps. The circuits of choice are readily available low voltage linear regulators, controlled with an external voltage. The voltage $V_{ASIC3V9}$ is supplied from a simple LM317 with a appropriate resistor combination. In order to monitor the currents of $V_D$, and $V_{SSS}$ I chose the regulators LT3042 and the LT3090, both being low noise, externally adjustable linear regulator from Linear Technologies.
The schematics of the regulators are in the appendix, and component placements and values can be read up in readiliy available, well explained datasheets. The control voltages $V_{CURR}$, $V_{REF}$, $V_{TH}$ and $V_{BW}$ only require very little current, so it's easiest to drive them from the DAC output. Using the DAC6578, it's necessary to add an RC low pass filter with a 10kΩ resistor and 100nF capacitor, in order to keep the ETTORE output stable. Without the low pass filter the ETTORE output oscillates with a frequency of 50kHz and an amplitude of 20mV. The reason why this happens has not been found.

## 5.4. Buffer Amplifier

### 5.4.1. Buffer Requirements

The buffer amplifies the signal from the ETTORE, to properly drive the ADC. The ETTORE is only able to provide little current so the buffer needs to have a high impedance input. It should have a bandwidth of at least 30 MHz, in order not to slow down the signal rise time of the detector. The gain of the buffer should be between 1 and 2 - depending on the input range of the ADC. The ETTORE preamplifier has a maximum dynamic output range of 2V. Assuming an operating dynamic range of 2V and a buffer with gain $G = 2$, the buffer output dynamic range is 4V. With a series output

resistance of 50Ω used with an ADC input resistance of 50Ω, the buffer can drive an ADC with a 2V amplitude. If the buffer is used to drive a high impedance ADC, the ADC needs to have with an input range from 0 - 4V.
The buffer needs to have an offset voltage control - which determines the reference point $U_{offset}$, from which the input voltage $U_{in}$ is amplified:

$$U_{out} = G \cdot (U_{in} - U_{offset})$$

### 5.4.2. Buffer Schematic and Operation

A signal amplifier stage, with a unity gain buffer (UA1), and an inverting amplifier with gain $G = -R4/R3 = -2$ are shown in figure 5.12. Both amplifiers are very high speed LTC6229 OpAmps. The amplifier (UA1) decouples the ETTORE from the 500Ohm load of the amplifier (UA2). Allowing the ETTORE to directly drive the amplifier (UA2) with a high input resistance (R3), would decrease the bandwidth of the amplifier, below an acceptable value. It's necessary to use small resistor values, in order to keep the bandwidth high, as in combination with parasitic board capacitances the bandwidth would drop. Furthermore, high speed OpAmps are in danger of producing an oscillations at the output. Minor board capacitances in the range of 1 - 2pF between the negative input and ground would introduce phase shifts between the inputs, leading to oscillations. The capacitor (C3) mitigates this problem by limiting the bandwidth of the amplifier. Potentially it would be possible to reduce the capacitor (C3) to a value of 2.5pF - 4pF. The transistor (Q1) shortcuts the output of the ETTORE, activating a 'channel disable' feature within the ETTORE, and disabling it's influence on the generation of the global 'saturation reached' signal.

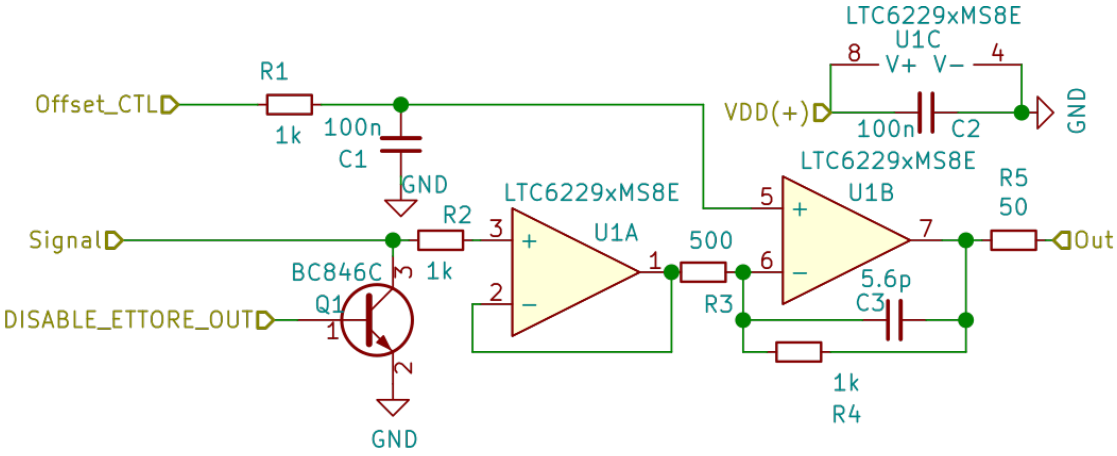



**Figure 5.12.:** The schematic of the high speed inverting amplifier with offset.

### 5.4.3. Buffer Bandwidth Measurement

The simulated frequency response of the buffer amplifier is shown in figure 5.13. Simulating with different (C3) values, ranging from 4.5pF to 6pF, a spread over 10MHz of the buffer bandwidth is visible, as indicated by the two black arrows in the 3dB region. The measured response is shown in figure 5.14. The values for the bandwidth match very well $\approx 35\,\text{MHz}$, and as indicated by the markers in the measured response, the gain is also correct – a gain of 6dB corresponds to $G = 2$.

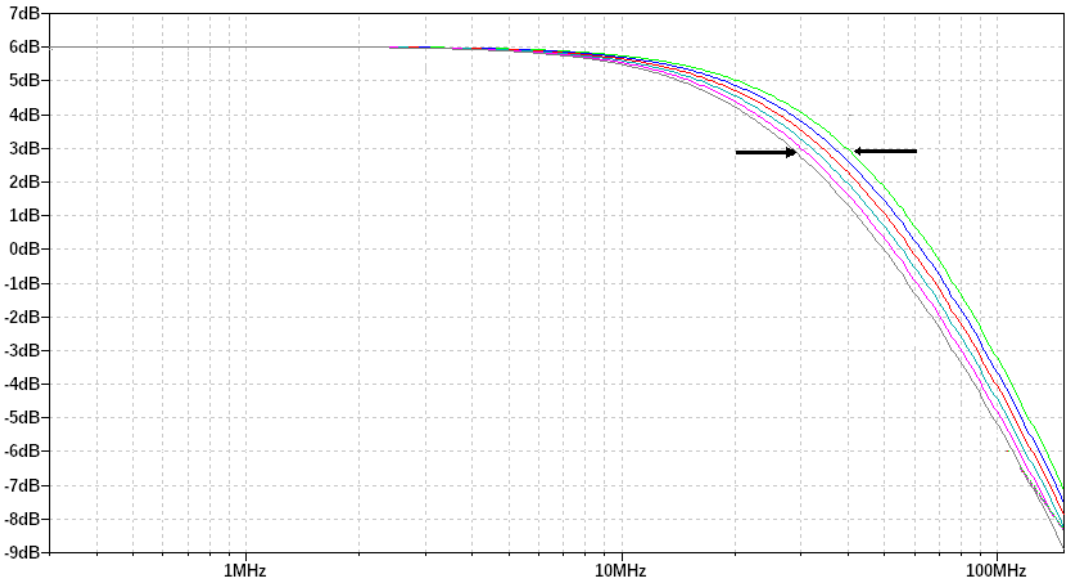



**Figure 5.13.:** Frequency response of the amplifier shown in figure 5.12, simulated in LTspice. The two arrows indicate the buffer bandwidth spread from 30 MHz to 40 MHz, when (C3) changes from 4.5pF to 6pF. This is of interest, as capacitor production tolerances are rather large for small valued capacitors.

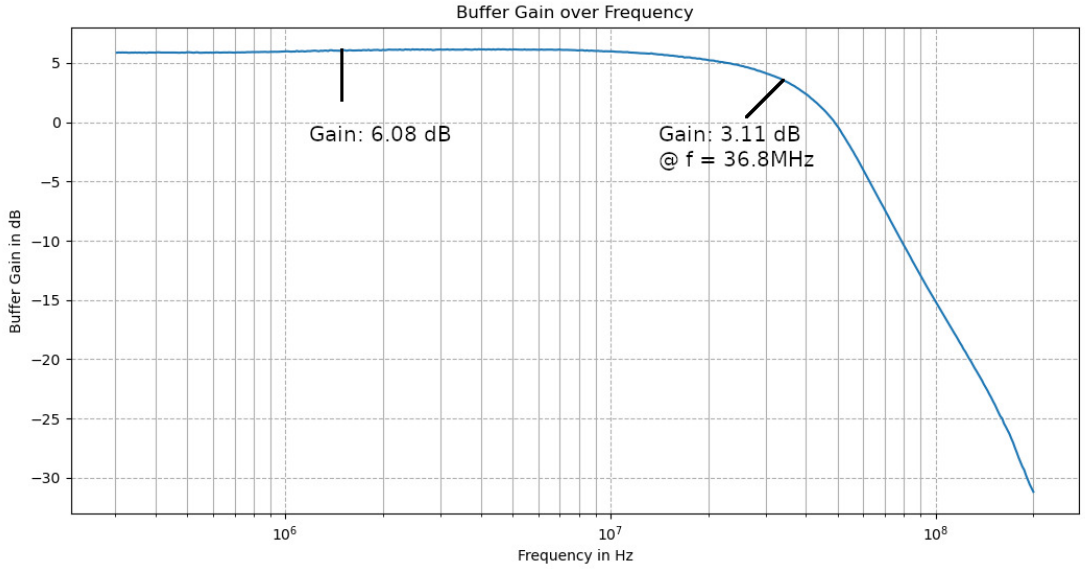



**Figure 5.14.:** The measured frequency response of the amplifier shown in figure 5.12.

### 5.4.4. Buffer Crosstalk

Crosstalk between two amplifiers is an undesired effect happening between two neighboring amplifiers, and is a measure of how much of the input signal of one amplifier leaks to the output of the other amplifier. This leakage is usually a capacitive or inductive coupling through either cables or long parallel PCB traces.
Crosstalk between detector pixel channels would distort the energy measurement, and lead to a distortion of the differential $\beta$-spectrum. Therefore it's of interest to know how strong the crosstalk is.
It is measured by feeding a signal with a known frequency and amplitude, while measuring

the other amplifier output at that known frequency. For the measurement only one offset voltage reference was providing 'Offset_CTL' for both buffer channels. The measured crosstalk between to buffer channels is shown in 5.15 and is at most −53.4 dB at the frequency of 6.54 MHz. The peak like resonance in the crosstalk can be caused by the self resonant frequency of the (C1) capacitor. With current detector related crosstalk, this is an acceptable value corresponding to a signal amplitude ratio of 1 to 467. In our current prototype setup we experience a detector related crosstalk with an amplitude ratio of at least 1 to 15, between two neighboring pixels [31].

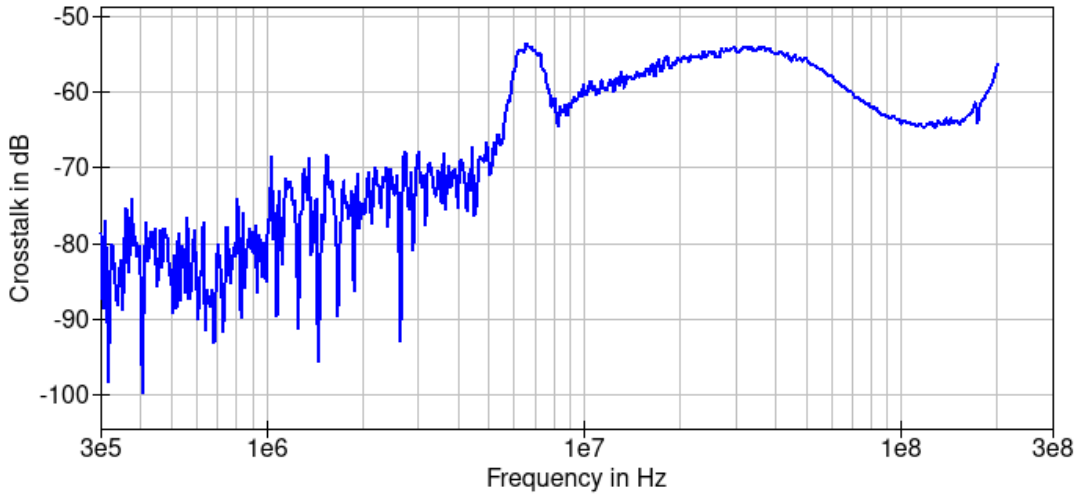



**Figure 5.15.:** The measured crosstalk between two buffer channels, with the offset voltage being provided by only one reference 5.12. The maximum crosstalk is at −53.4 dB at the frequency of 6.54 MHz

### 5.4.5. Buffer Step Response

**Notes on Operation** The amplifiers can only process inputs that are 1.2 V below the positive supply rail, as the inputs of the OpAmp are a differential PNP transistor pair. When, for example supplied with 4 V, the amplifiers can only process input voltages of up to 2.8V properly. Input voltages above this voltage distort the gain of the amplifier, and lower the bandwidth. The danger lies in signals that 'look' alright on the oscilloscope, but are distorted due to incorrect input range.

**Alternative OpAmp for Reducing Heat Dissipation** When regarding the same circuit, and looking for parts replacement, the LTC6227 is a pin-compatible replacement, which requires only one third of the supply current of LTC6229. (5.5mA/channel vs. 16mA/channel). It has the advantage of lower heat dissipation, at almost the same amplifier bandwidth. In the 48 channel buffer design, I haven't taken the heat dissipation into account, and the board heats up considerably - to a temperature, where it's just tolerable to touch the PCB. Using the LTC6227 would be an improvement in this regard.

**Alternative Buffer Architecture** An alternative schematic for the buffer is a noninverting amplifier with offset, as shown in figure 5.16. It is critical, that the amplifier U1B is a high speed amplifier, to properly react to load changes at the resistor (R1). In prior experiments I have made the error and used a slow amplifier, which lead

to unacceptable ringing in the step response signal. Being discouraged by these results I stuck with the inverting amplifier. Note, that the architecture looks very similar to the input of an instrumentation amplifier. The operational equation of the amplifier is:

$$U_{\mathrm{Out}} = (1 + \frac{R_2}{R_1}) \cdot U_{\mathrm{In}} + U_{\mathrm{Offs}} \cdot \frac{R_2}{R_1}$$

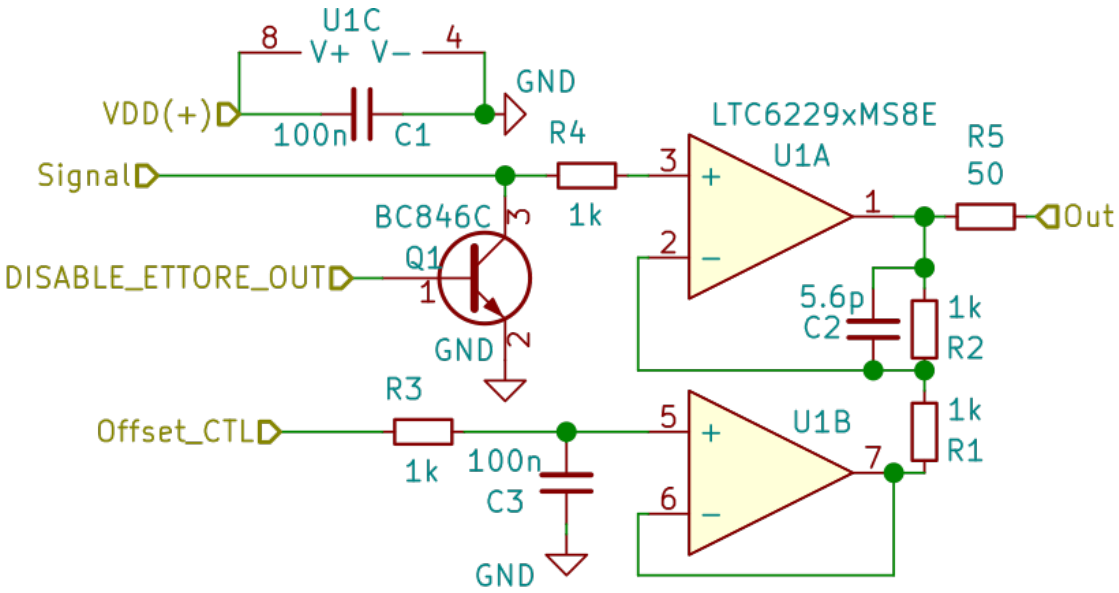



**Figure 5.16.:** An alternative schematic for the buffer, a noninverting amplifier with an offset, provided by (U1B).

### 5.4.6. Buffer Hardware Iterations

Here I list the buffers that I have built. There was one noninverting amplifier version in figure 5.17, which had a non satisfactory step response with too much ringing, caused by the choice of a wrong amplifier. Then I had built a 2 channel version of an inverting amplifier, shown in figure 5.18, which went on the final 48 channel board, shown in figure 5.19.
For cross checking the buffer performance, I have also built a 7 channel unity gain buffer, to investigate the detector resolution. This unity gain buffer is shown in figure 5.20.

## 5.5. Building the Schematics

**Design** The schematics and the PCB files were created in KiCad 5 - a high quality, open source circuit CAD suite. For building schematics with analog signal frequencies above several MHz, it's necessary to have a board with a continuous ground plane, in order to reduce electromagnetic radiation, and crosstalk. With 48 channels in a dense space, it's necessary to have a 4 layer board.

### 5.5.1. Hardware Iterations

I went through several hardware iterations of the regulator, the reset generator and the buffers, which I would like to document here:

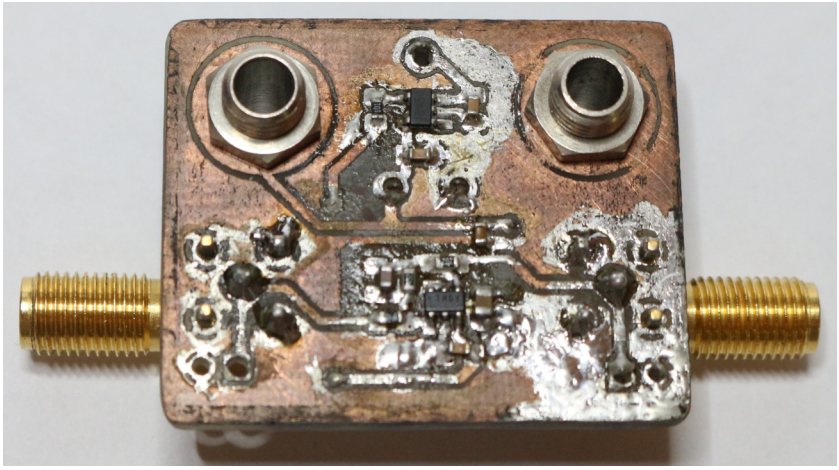


**Figure 5.17.:** A prototype buffer amplifier, with too much ringing on the output.

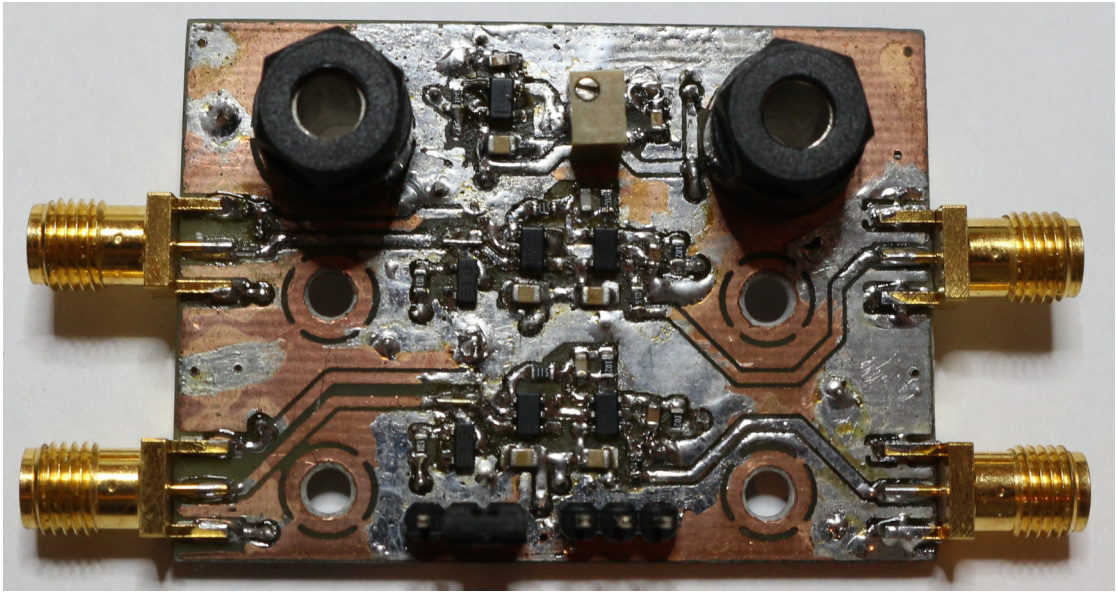


**Figure 5.18.:** A two channel amplifier prototype board, each amplifier as drawn in schematic 5.12

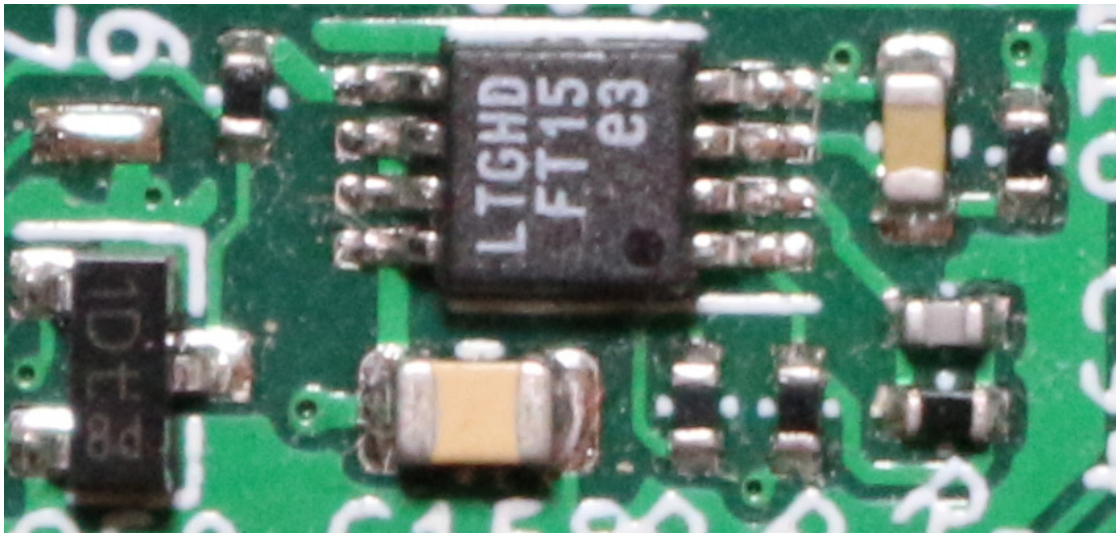



**Figure 5.19.:** A single amplifier, as drawn in schematic 5.12, and replicated 48-fold on the 48 channel buffer board.

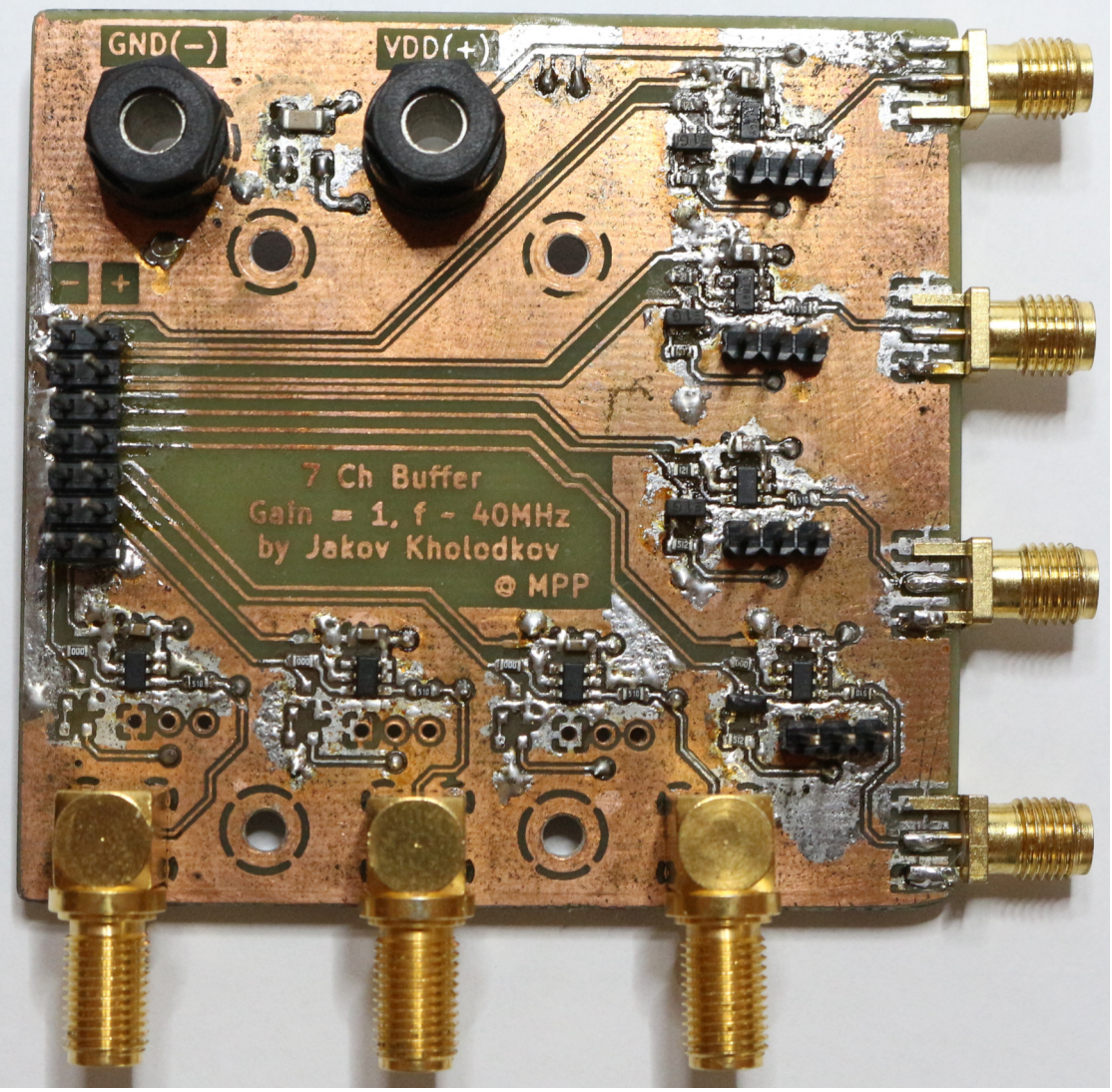



**Figure 5.20.:** A 7 channel unity gain buffer for testing the detector energy resolution with buffer gain 1 results are shown in 6.10. Four channels on the right have a populated transistor, to test the 'channel - disable' feature of the ETTORE.

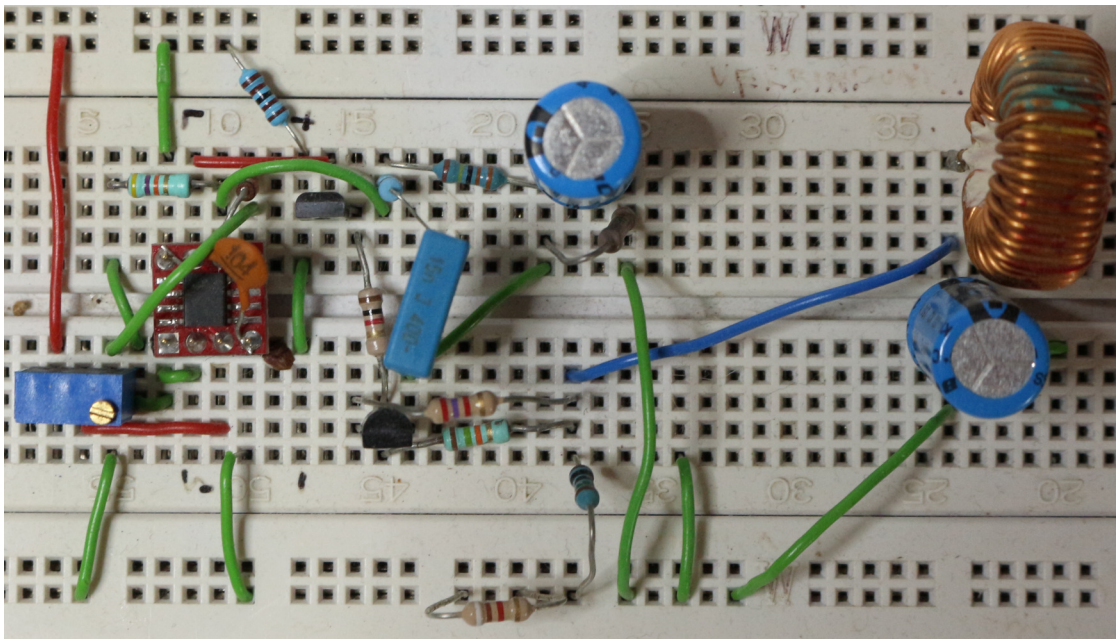


**Figure 5.21.:** Prototype of the sinking linear regulator, build on a breadboard. Breadboaring works well with low voltages at low frequencies, and when pickup noise plays no major role in the system. When working with a very low power high voltage supply, and small capacitors, the biggest danger is just risking a zap. The ring inductor is for filtering switching noise from the high voltage power supply.

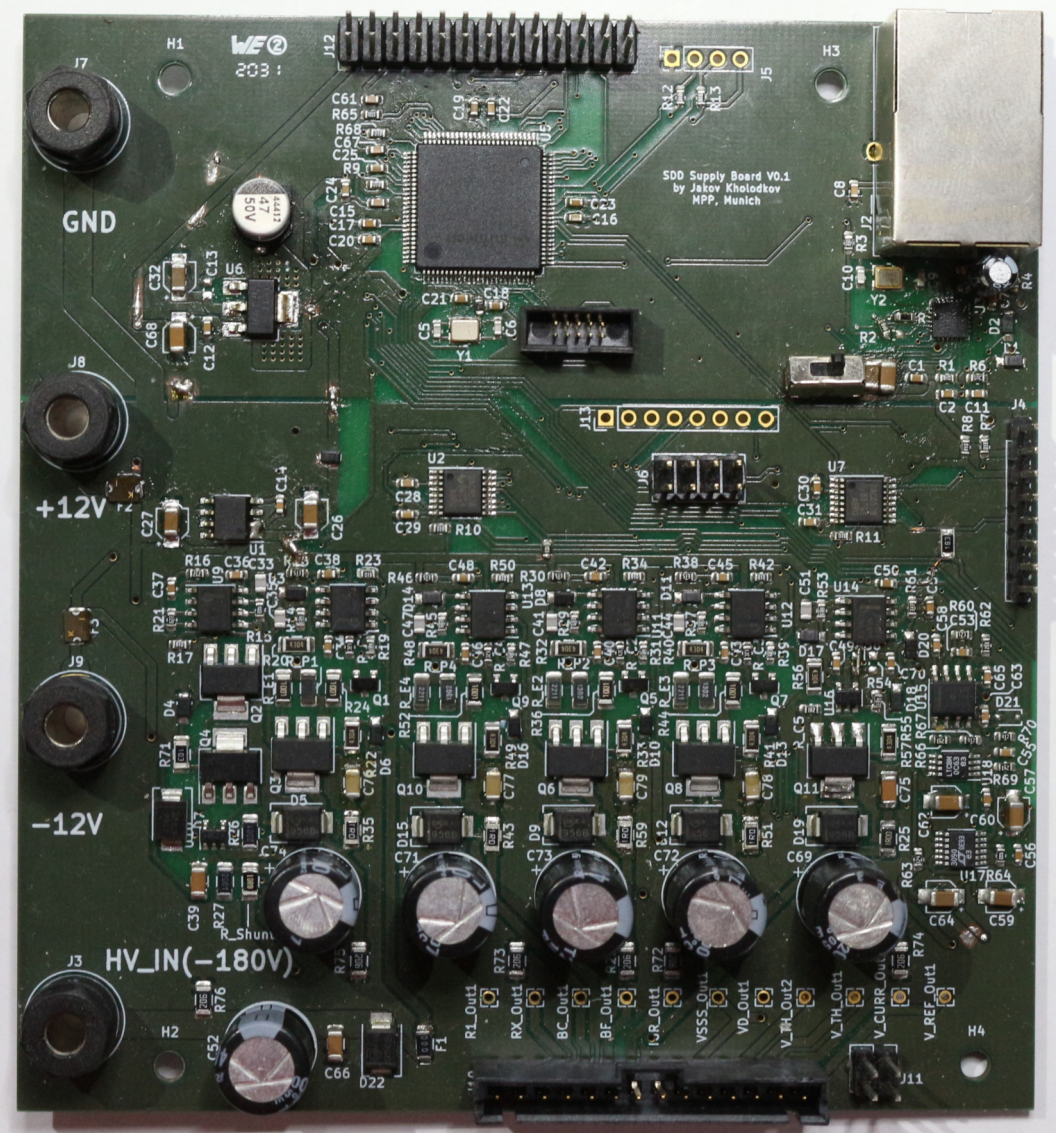



**Figure 5.22.:** This is a prototype, that supplies all high and almost low voltages to the detector board. Exceptions are the $V_{ASIC3V9}$ and the RESET signal. This was used to test the viability of the high voltage regulators. The low voltages were supplied by a digital to analog converter (DAC), and two linear regulators.

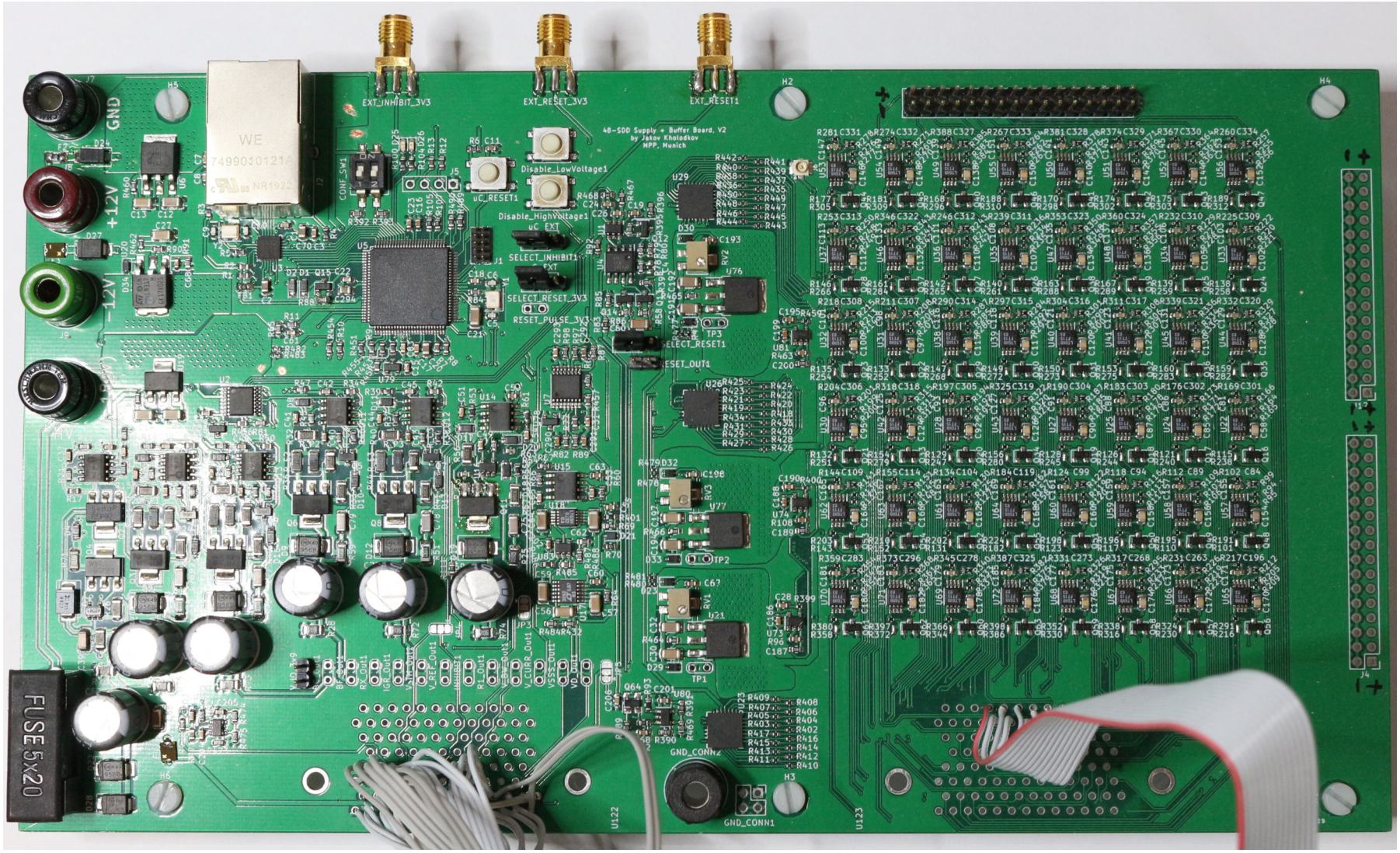



**Figure 5.23.:** The most recent development: a full board with all high voltage and low voltage supplies, a reset generator and 48 buffer channels.

The following images are sub-schematics as explained above, from the 48 channel board.

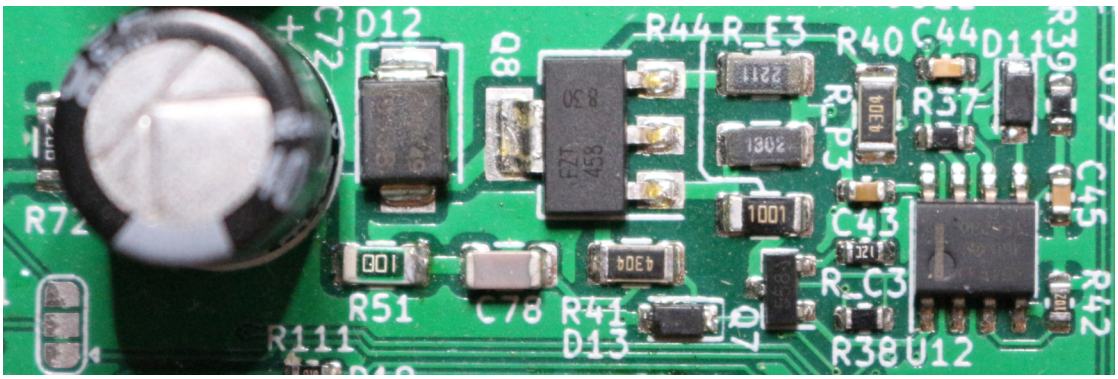



**Figure 5.24.:** The high voltage linear regulator 5.8, without the current monitoring capability. The current monitor requires approximately the same PCB space as the linear regulator with high voltage monitoring.

# Chapter 6.

# Hardware Performance Measurements

To measure a potential sterile neutrino signal, a detector resolution of at least 500eV is required. [24] The performance of the designed system is evaluated by measuring the achieved detector resolution on x-rays from a $^{55}$Fe source, and by comparing this resolution to the existing setup from XGLAB.

## 6.1. The Existing System from XGLAB

The existing system, shown in figure6.1 developed by the company XGLAB has been used many times in our experiments, and it's a very good setup, which sets high standards. From here on I refer to this setup as 'XGLAB signal chain'.
The only drawback of the XGLAB signal chain are the switched mode DC/DC converters for the detector power supply. These DC/DC converters use solid core transformers which are not allowed for the high magnetic field environment at the spectrometer.

## 6.2. The Thesis Measurement Setup

The 48 channel board was the last development, and has not yet been successfully set up to capture $^{55}$Fe spectra. For performing the measurements, the prototype power supply shown in figure 5.22 and the buffer shown in figure 5.18 were used. A block diagram of the thesis measurement setup is shown in figure 6.2. Measurements were also taken with the 7 channel unity gain buffer, and are shown in section 6.8. Each of the components was on separate boards, in an aluminum shielded box. The figure 6.3 shows the setup with the power supply board in the bottom right corner, and the 7 channel unity gain buffer board in the top left.

## 6.3. Detector Resolution Measurement

X-Rays from a $^{55}$Fe source are a good way to measure the resolution of the detector system, as $^{55}$Fe sources are readily available, deliver a high count rate and only emit x-rays.
A recorded $^{55}$Fe spectrum with the S0-7-2 TRISTAN detector and the prototype setup with a gain 2 buffer is shown in figure 6.4. The spectrum shows the K-$\alpha$ and the K-$\beta$ peak of the $^{55}$Fe source, at 5.895 keV and 6.490 keV. The visible peaks are comprised of 3 and 4 sub-peaks, only visible as one. By using the known position of the peaks, it's possible to calibrate the spectrum and calculate the full width half maximum (FWHM) of the peaks in eV. The visible spectrum was recorded with a peaking time of 5.76 $\mu$S. The detector S0-7-2 does not reach the aforementioned ideal 140 eV resolution, because it was not cooled, and the waver charge it came from was off specification.

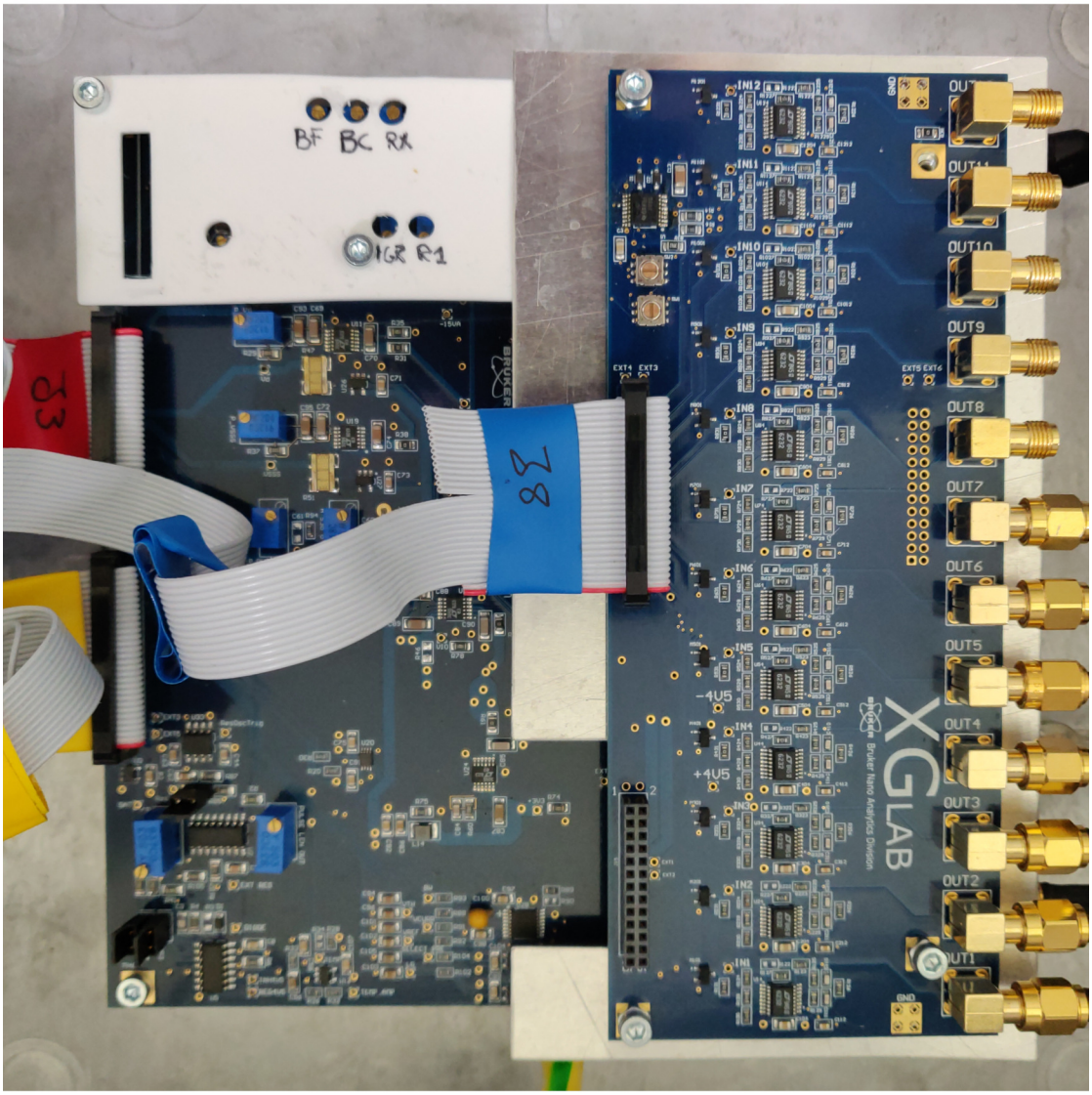



**Figure 6.1.:** The bias Board form XGLAB consisting of two PCBs, the top PCB is the buffer section, the bottom PCB is for the high and low voltage power supply, generating the RESET signal, and monitoring currents.

## 6.4. Resolution Dependence on Peakingtime

The energy resolution varies with the peaking time of the trapezoidal filter. At low peaking times, the resolution improves with increasing peaking time, as the averaging property of the filter suppresses noise.
With further increase of peaking time, the resolution decreases due to current noise within the detector. This behavior is visible in figure 6.5, where the measurement was performed with one pixel of the detector S0-7-2 and the XGLAB signal chain, measuring $^{55}$Fe x-rays.

## 6.5. Comparing the Resolutions at Different Peakingtimes

The plot 6.6 shows the comparison of the energy resolutions of $^{55}$Fe K-$\alpha$ lines with different signal chains. The worsening of the resolution is caused by an oscillation in the

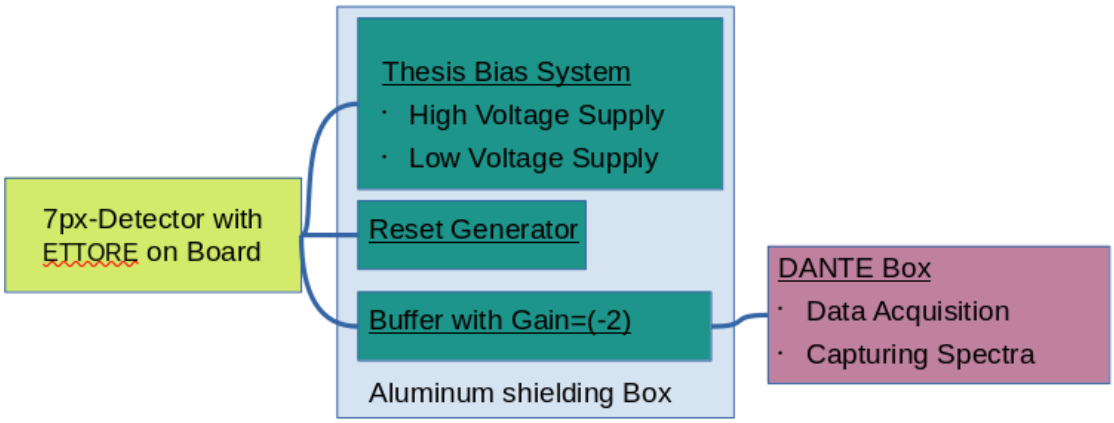



**Figure 6.2.:** The measurement setup for the following measurement results.

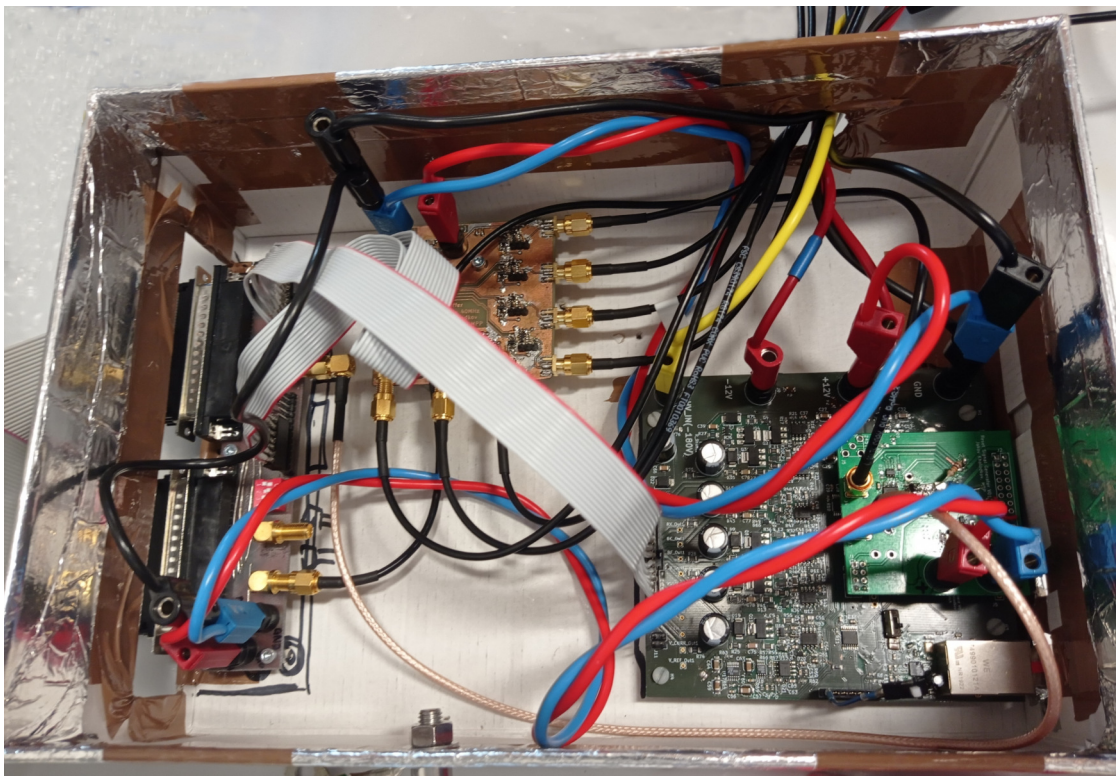


**Figure 6.3.:** The prototype setup with a unity gain buffer in an aluminum shielding box.

internal 3.3V supply line of the bias board. Further details are explained in section 6.9.

## 6.6. Comparing the Noise Power Spectral Densities

Analyzing the frequency components of the detector signal provides another analysis tool, which can help identify noise sources and oscillations which not directly visible with the oscilloscope. Figure 6.7 shows the power noise spectral density $W(\omega)$ from each of the setups. $W(\omega)$ is calculated by applying the Welch transform to the detector signal, as shown in 3.6 on page 9. The general rule is, that the lower the noise components between $\sim 100\,\text{kHz}$ and $1 - 3$ MHz, the better the resolution of the energy peaks. The average

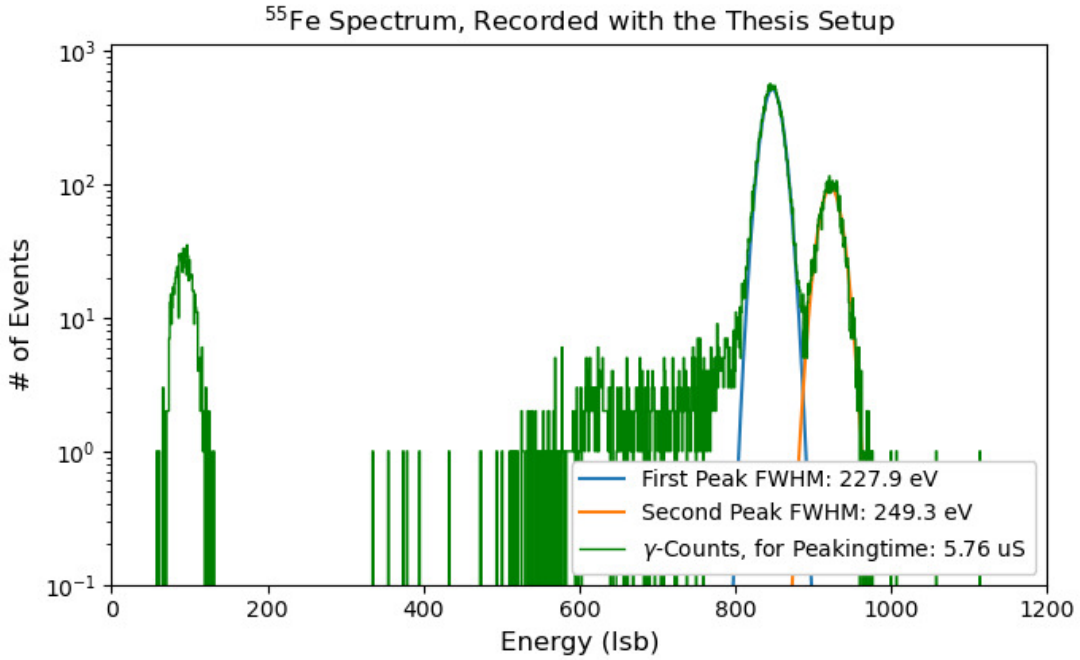



**Figure 6.4.:** An example spectrum of a $^{55}$Fe source, measured with the TRISTAN detector. The resolution is measured by evaluating the FWHM of each of the peaks.

height of the power spectral density is dependent on the rate incoming x-ray events, and the reset pulse frequency, the frequency at which the detector anode is flushed from charge. The higher the event-rate, and the higher the reset pulse frequency, the higher the power noise spectral density.
The thesis signal chain result, shown in blue, has a peak at $\sim 250\,\mathrm{MHz}$, which causes the bump in the resolution sweep figure 6.6. This peak has the effect of lowering the resolution in the region of interest, as shown in the following section. The XGLAB signal chain result, shown in orange, performs better in the region of interest.

## 6.7. Calculating a Resolution Sweep from the Noise Power Spectral Density

Each point of the peakingtime sweep as shown in 6.6 is dependent on how much noise is in the signal, and on the trapezoidal filter. When processing the detector signal, and the trapezoidal filter signal in the frequency domain, one can directly estimate the form of the peakingtime sweep by calculating the time averaged variance:

$$\sigma^2 = \int_0^\infty W(\omega) \cdot |H(\omega)|^2 \mathrm{d}f \tag{6.1}$$

where $W(\omega)$ is the noise power spectral density, plotted in 6.7, and $H(\omega)$ the frequency response of the trapezoidal filter. After evaluating this integral with different trapezoidal filters, the resulting curve 6.8 shows resemblance between the resolution sweep in figure 6.5, especially with regard to the position of the resolution worsening bump.

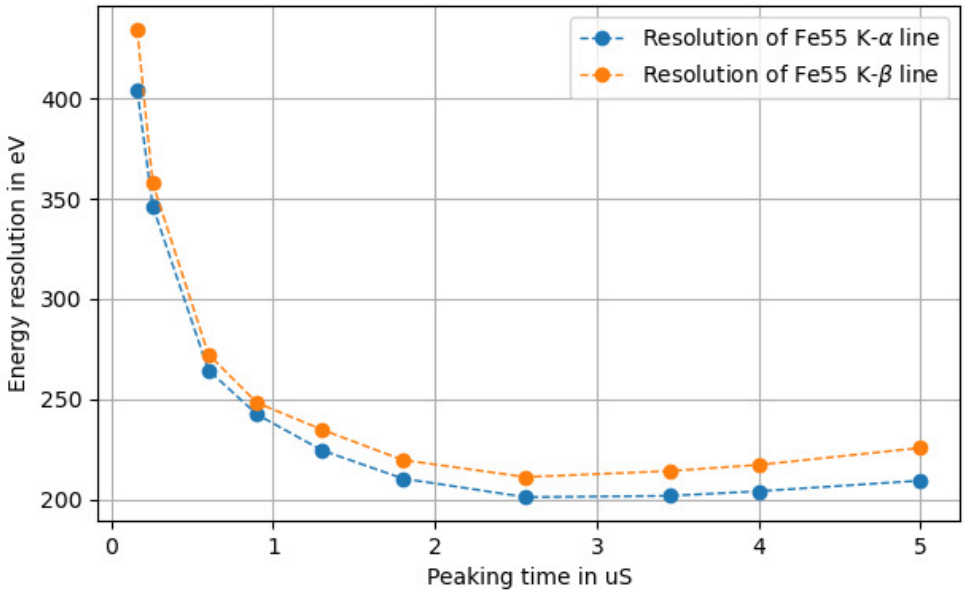



**Figure 6.5.:** Blue and yellow lines represent the energy resolution of the K-$\alpha$ and the K-$\beta$ peak in the spectrum. The resolution sweep of the S0-7-2 detector, pixel 6, measured with the XGLAB signal chain at room temperature, showing an optimum filter peaking time of 2.5$\mu$S.

## 6.8. Resolution Sweep with a Unity Gain Buffer

Out of experimental curiosity, I have build a unity gain buffer to test whether it's necessary to use a buffer with gain=2. The following images show an acquired spectrum 6.9, a spectrum resolution sweep over peaking time in figure 6.10, and event steps in 6.11a. The resolution worsening bump in the peaking time sweep is still visible, which hints to a cause in the power supply section. When comparing the event steps, the signal to noise ratio of the signals looks very similar, if not a little better with the unity gain setup. Nevertheless, the XGLAB setup achieves better resolution results. This might either be an experimental error – or the cause of a yet unknown problem. Either way, this topic might be worth further investigation.

## 6.9. Power Noise Spectral Density Measurement with the 48 Channel Bias and Buffer

I performed a measurement of the power noise spectral density of the detector with the 48 channel bias and buffer from figure 5.23. On the first attempt, the result was very similar to what is shown in figure 6.7, there was a spectral noise peak at approximately 250 kHz. For monitoring the high voltages, the micro-controller has a build in ADC, which causes the oscillation. When the ADC is not supplied with power, the oscillation on the 3.3V supply line stops. I found this by cutting the PCB supply trace of the ADC. The measured spectral noise power density and the derived shape of the average noise powers at different peaking times are shown in figures 6.12 and 6.13. The plot of the spectral noise power density shows a comparable performance of the 48 channel buffer and bias board to the , almost reaching the noise level of the XGLAB signal chain. This translates to very similar noise levels at different filter peakingtimes. At filter

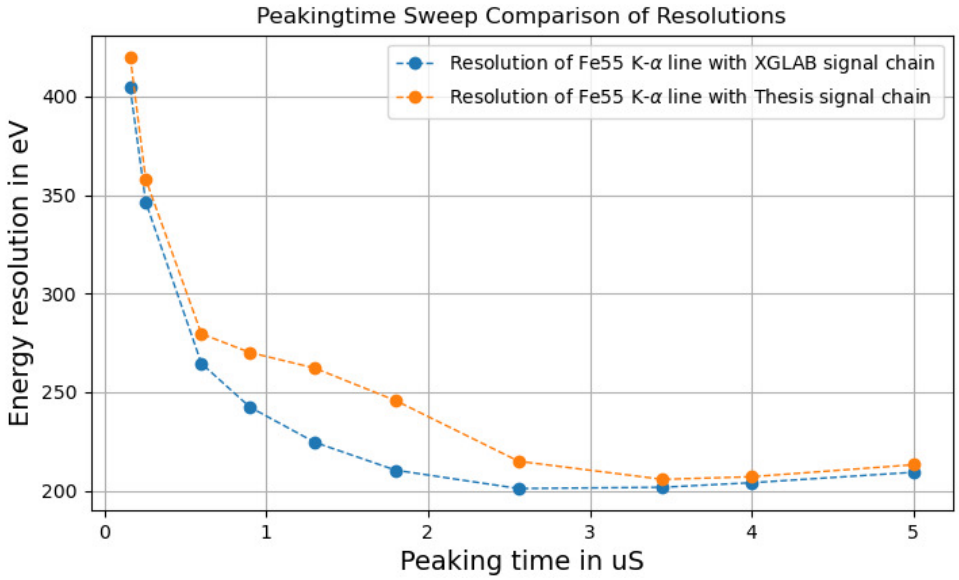



**Figure 6.6.:** (Blue) shows the energy resolution sweep with the XGLAB signal chain. (Yellow) shows the energy resolution sweep with the signal chain developed in this thesis. The yellow line shows a worsening of the resolution in the region from 0.5 - 3 $\mu$S.

peakingtimes below 1 $\mu$S the noise levels are the same, and deviate slightly at longer filter peakingtimes. With the nominal event rate at the detector of $10^5$ electrons per second, a filter peakingtime of 1 $\mu$S is planned. Regarding these settings, the 48 channel bias and buffer board could be used.

## 6.10. Conclusion

With the signal chain developed in this thesis, the detector resolution is close to what can be achieved with the XGLAB signal chain. The cause for the bump like structure is found and can be eliminated. The high voltage temperature dependent fluctuations shown in figure 5.10, seem to worsen the overall resolution of the setup by a few eV.

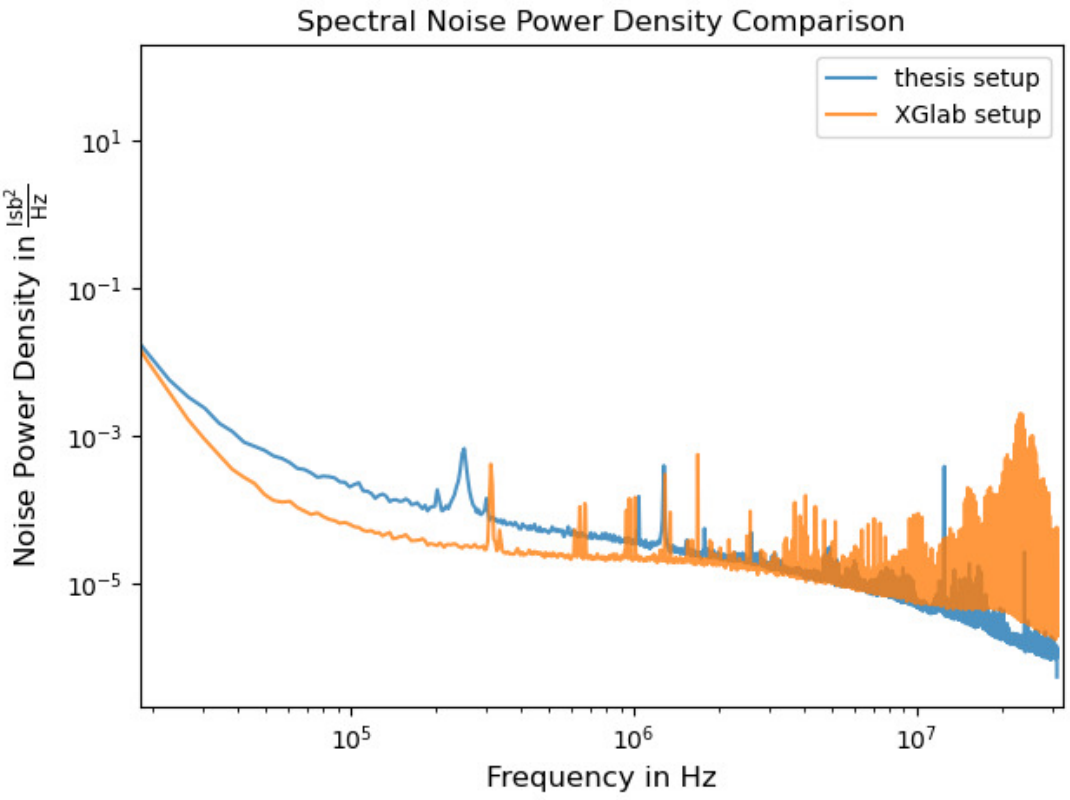



**Figure 6.7.:** Plot showing the frequency components of the detector signal, with two different setups.

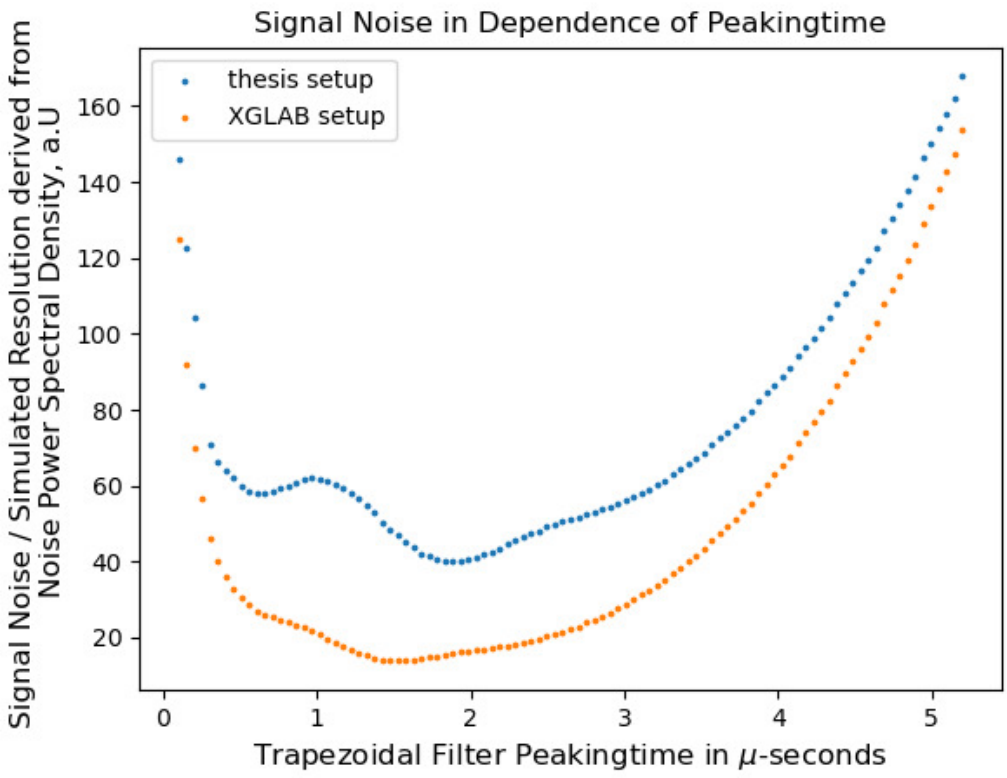



**Figure 6.8.:** Plot showing the calculated signal variance at different filter peakingtimes. There's a resemblance between this curve, and the resolution sweep in figure 6.5.

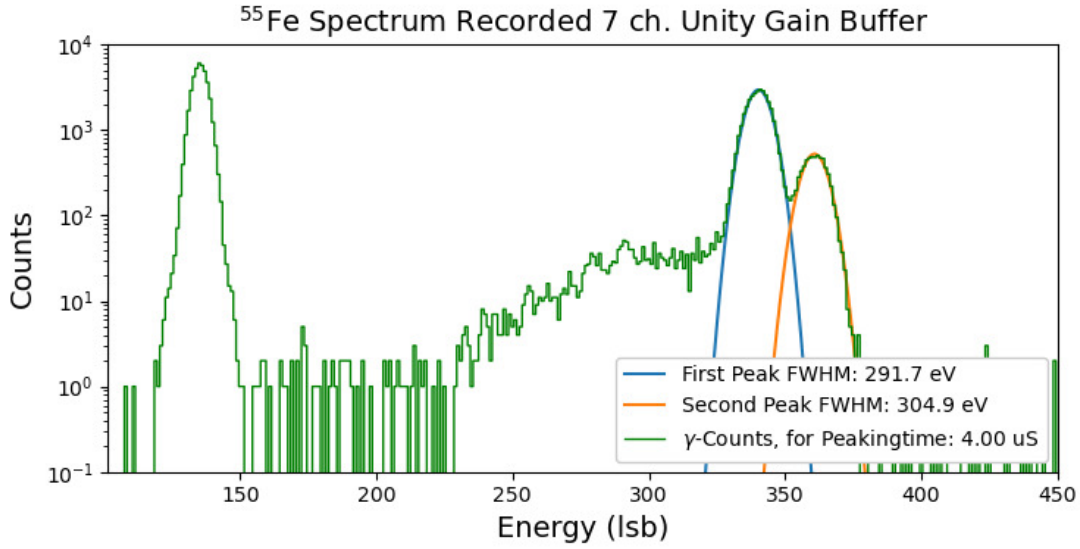



**Figure 6.9.:** An $^{55}$Fe spectrum captured, with the prototype setup and the unity gain buffer. Note that the binning is smaller in comparison to 6.4, as the XGLAB Buffer has gain = 2. Even though the step responses of the buffers look very similar (figure 6.11b and 6.11a), the resolution is significantly worse.

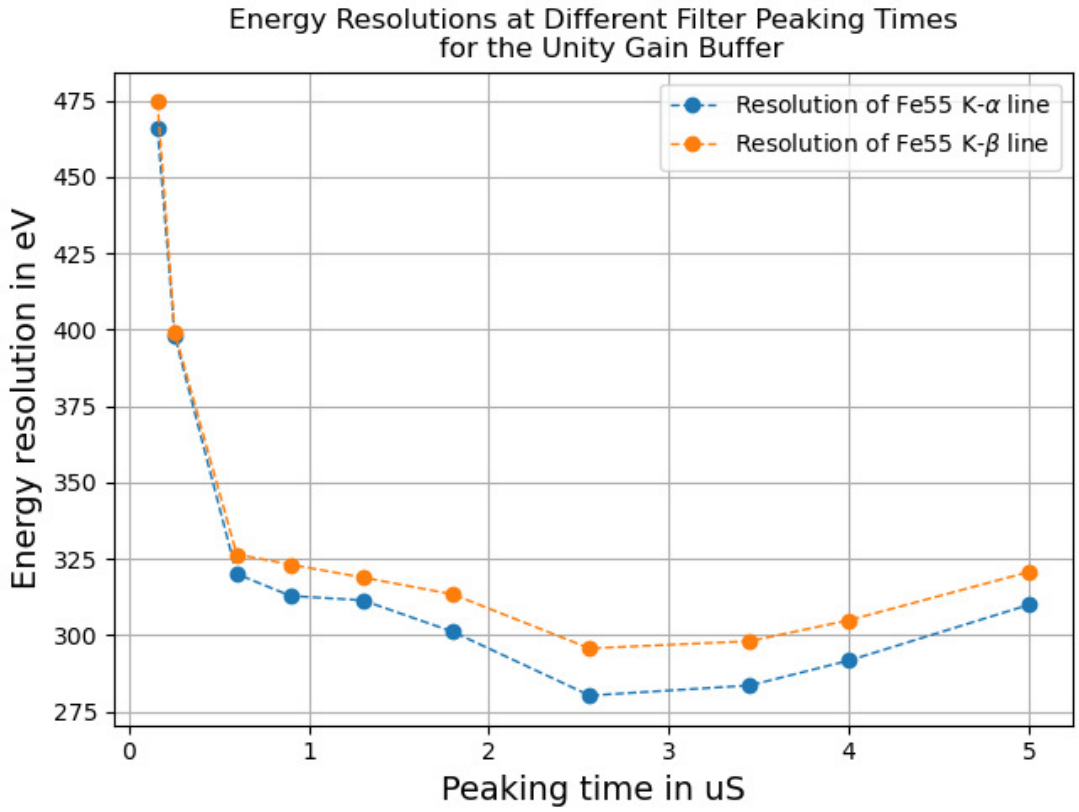
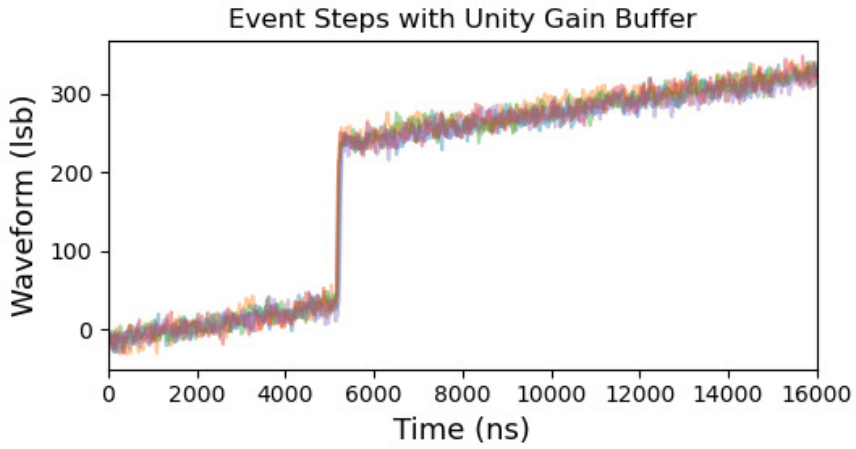
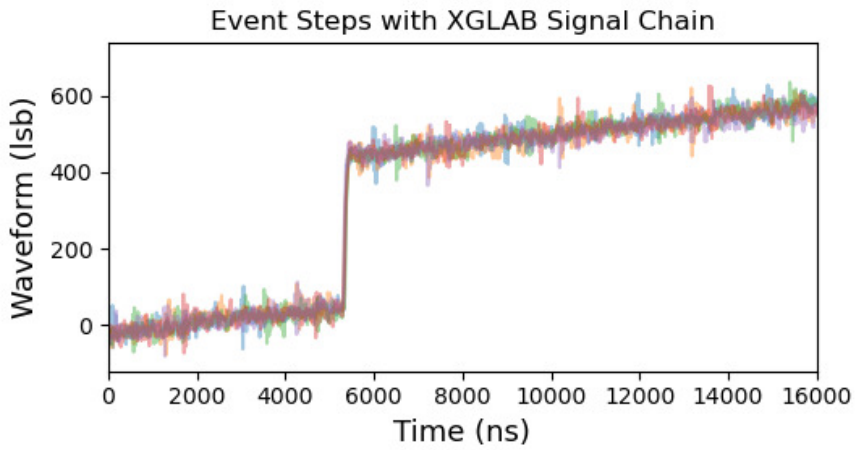



**Figure 6.10.:** The image shows the energy resolution sweep when using the linear regulators and a unity gain buffer shown in 5.20




**(a)** Event steps with the thesis setup, and a unity gain buffer. Note the different scale between the XGLAB steps and the unity gain buffer steps.




**(b)** Event Steps with the XGLAB buffer for optical comparison. High frequency noise on the signal gets filtered out.

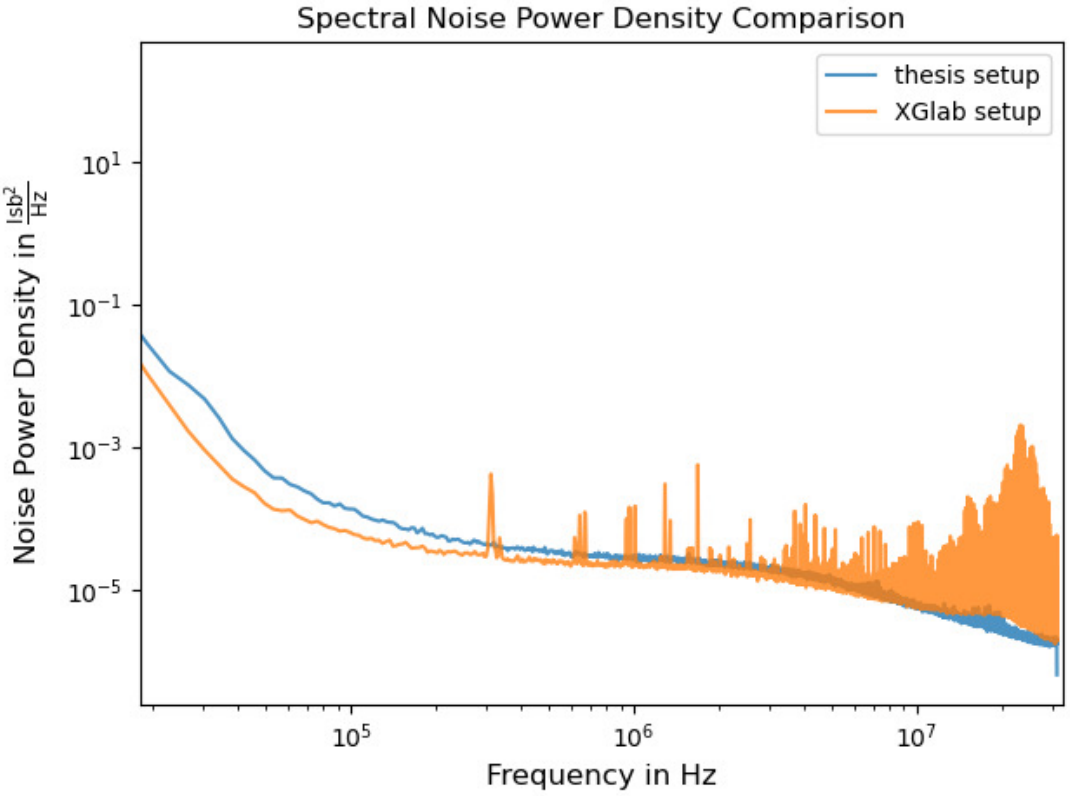



**Figure 6.12.:** Noise power spectral density for two different setups: the XGLAB signal chain, and the 48 channel buffer and bias board. The plots show little difference in noise densities in the region of interest. At higher frequencies the XGLAB signal chain exhibits higher noise levels due to switching noise of the internal DC/DC converters.

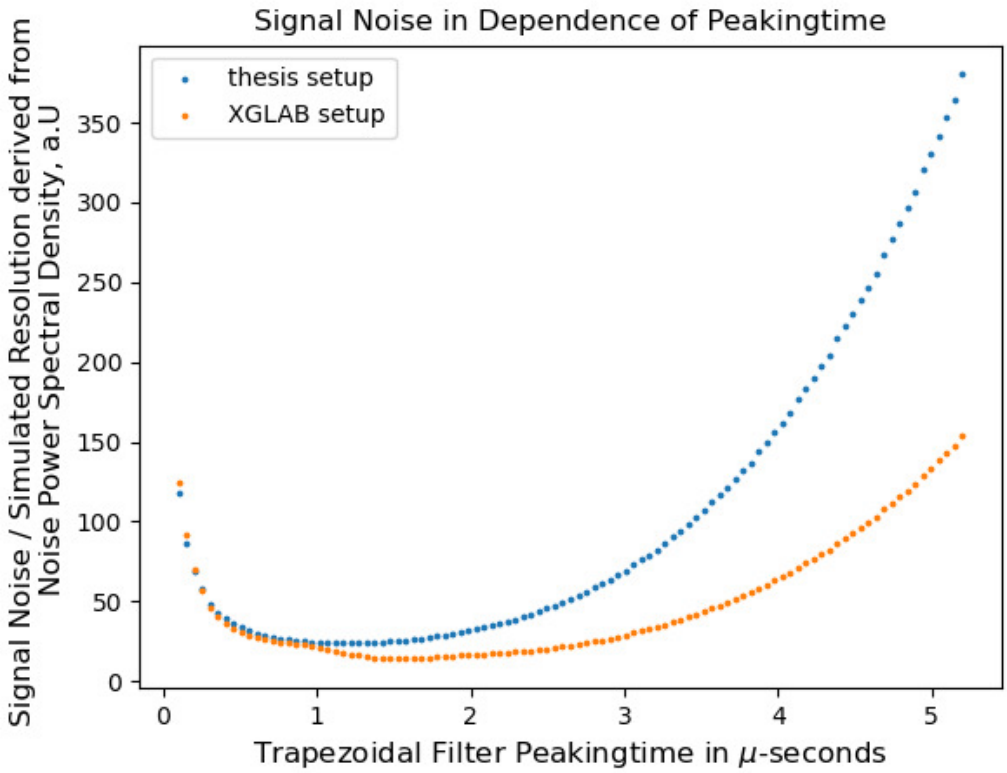



**Figure 6.13.:** The noise power at different filter peakingtimes for two different setups: the XGLAB signal chain, and the 48 channel buffer and bias board.

# Chapter 7.

# Measuring ADC Nonlinearities

The ADC is required for digitizing the amplified detector signal, and is a key component of the signal chain. Kai Dolde shows in [13] that the integral nonlinearity of the ADC can lead to a significant distortion of the measured differential $\beta$-spectrum. He shows several ways to mitigate the problem, one of them being to mitigate the problem by correcting the nonlinearities introduced by the ADC. For those corrections it's necessary to precisely measure the shape of the nonlinearities of the ADC. In this chapter I will cover a practical approach of measurement and evaluation procedure of ADC nonlinearities.

## 7.1. ADC Transfer Function Errors

An ADC has a step like transfer functions, from an input voltage to a digital output code. Ideally this transfer function is a perfectly equidistant staircase, but due to manufacturing imperfections and different ADC architectures, the transfer function is slightly distorted. There are several types of distortion, as depicted in 7.1 and 7.2. The images show the

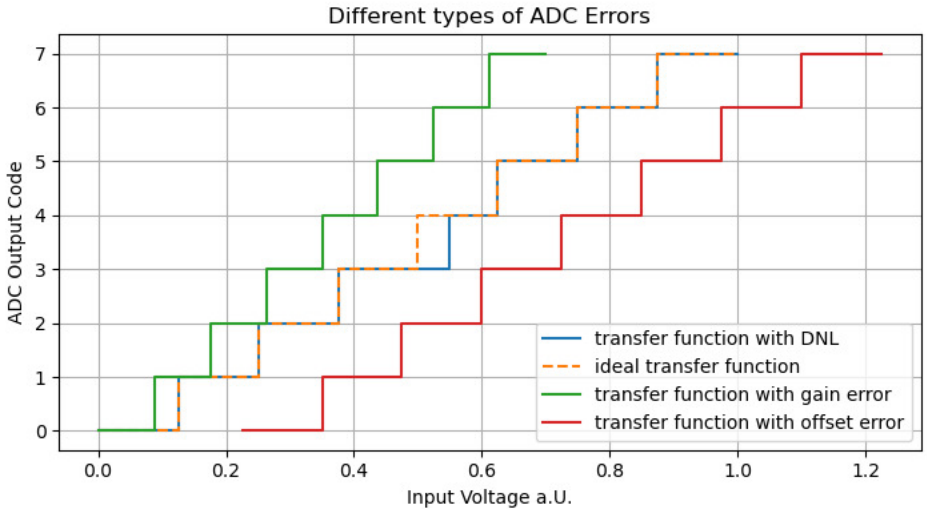



**Figure 7.1.:** An image with different ADC response functions.
(orange) shows an ideal ADC transfer function. (green) and (red) are functions with gain and offset error. (blue) shows a differential nonlinearity between the 3rd and fourth bit, which are both influenced by it.

ADC transfer function errors: offset error, gain error, differential nonlinearity (DNL) and integral nonlinearity (INL). Offset and gain error are easy to calibrate for, and don't matter for the measurement of the sterile neutrino. The differential nonlinearity is defined as:

$$\mathrm{DNL[i]} = \frac{U[i] - U[i-1]}{U_{(\text{eff LSB})}} - 1 \tag{7.1}$$

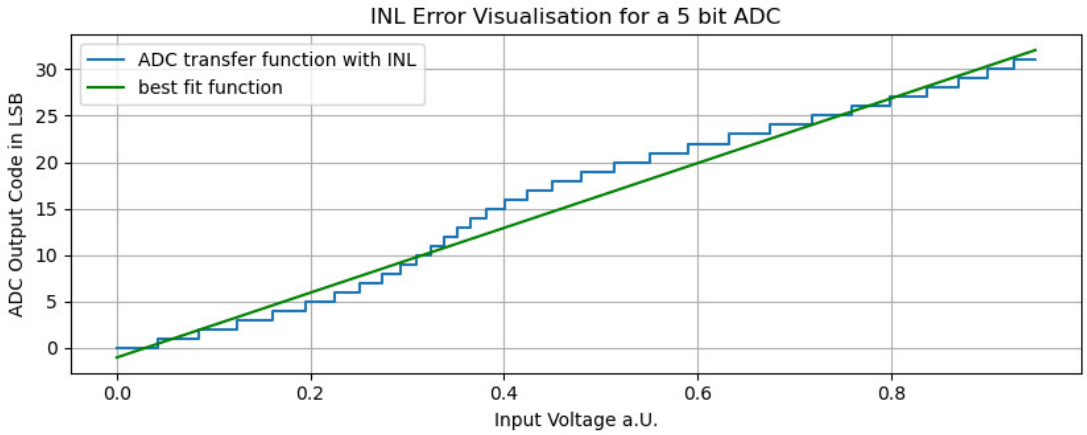



**Figure 7.2.:** A transfer function of a 5 bit ADC with integral nonlinearity. Integral nonlinearity is the deviation in LSB from the best fit function.

with $i$ being the output code, and $U[i]$ being the upper bound voltage, where the ADC outputs the $i$ as the output code. $U_{(\text{eff LSB})}$ stands for the effective voltage span of one least significant bit LSB, and it takes the gain error of the transfer function into account, such that

$$\sum_{i=1}^{N} \mathrm{DNL[i]} = 0$$

Where $N$ is the number of ADC Codes. This yields $U_{(\text{eff LSB})} = \frac{U[N]-U[0]}{N}$. For the DNL, only the error between two neighboring output codes is taken into account, and is a measure for how regular the staircase is.
The INL is the deviation from the measured ADC transfer function to the best fit line of the transfer function, in LSB:

$$\mathrm{INL[i]} = \frac{\mathrm{U_{measured}[i]} - \mathrm{U_{best\ fit}[i]}}{U_{(\text{eff LSB})}}$$

## 7.2. Measurement of ADC Nonlinearities

The measurement of ADC nonlinearities is done by feeding a known signal to the ADC over a long period of time and counting how many times an ADC output code appears. This is known as the ADC histogram technique. It's easiest to use a sine function as a known signal, because sine waves can be generated with very low distortion. In order not to distort the measurement of the histogram, one has to pay attention to the signal and sampling frequencies involved. In the measurement I used the CAEN V1782 14 bit ADC. The software of the CAEN card triggers a measurement and then records a window with a number of samples $S$. With such a windowed measurement one has to decide for a signal frequency, such that the signal has $C$ cycles per recorded window. For a uniform distribution of samples between 0 and $2\pi$, $S + 1 = n \cdot C,\ n \in \mathbb{N}$ must hold, which is fulfilled, if one has only one wave cycle across the record window. Furthermore the relation between the ADC sample frequency, and the sine wave frequencies must hold [8].

$$\frac{f_{ADC}}{f_{sine}} = \frac{C}{S} \tag{7.2}$$

When using only one sine wave cycle per record window, the equation 7.2 simplifies to:

$$f_{sine} = \frac{1}{t_w} \tag{7.3}$$

with $t_w$ being the record window duration in seconds.

## 7.3. Calculating the ADC Response from Measurement Results

The probability density function (PDF) of a sine/cosine wave with amplitude $A(t) = A_0 \cos(\pi t) + B$ is calculated by first finding it's inverse,

$$t(A) = \frac{1}{\pi} \operatorname{acos}\left(\frac{A - B}{A_0}\right) \tag{7.4}$$

and then deriving it

$$\mathrm{PDF}(A) = \frac{\mathrm{d}t}{\mathrm{d}A} = \frac{1}{\pi\sqrt{A_0^2 - (A - B)^2}}$$

Reading the derivative as: "the time spent in an amplitude interval dA" can help understand why this is the probability density function. A measured PDF is shown in figure 7.3. For this measurement, the 14 bit CAEN V1782 DAQ measured a sine wave from the Rhode&Schwartz SMA100B signal generator. I plotted histogram from the acquired wave snippets using a PC.

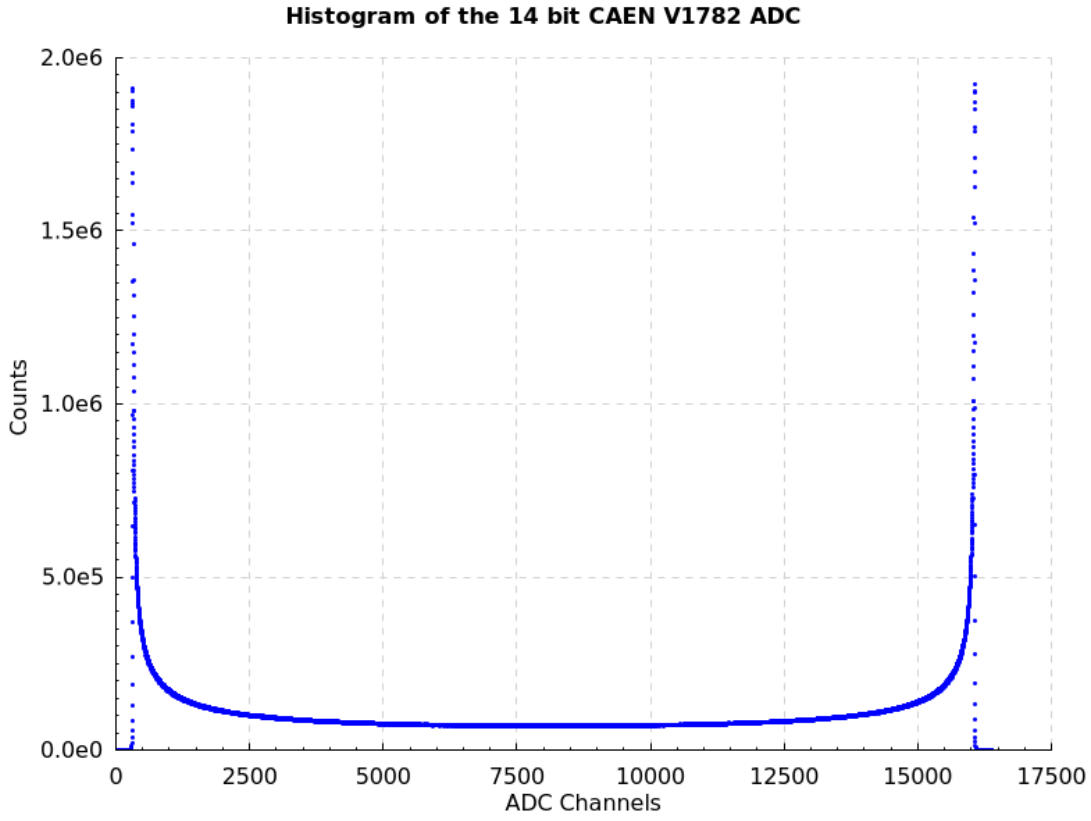



**Figure 7.3.:** The measured histogram, when feeding a sine wave to an ADC.

To calculate the ADC response function from this PDF, one calculates the discrete cumulative distribution function (CDF), $\mathrm{CDF(A[i])} = \sum_{j=0}^{i} \mathrm{PDF(A[i])}$ which is the discrete integral leading back to $t(A) = \frac{1}{\pi} \cdot \mathrm{acos}\,\frac{A-B}{A_0}$ from equation 7.4. In order to get the ADC response function, one has to solve for the voltage levels $u[i]$, where the ADC transitions happen, while normalizing the CDF:

$$u[i] = \frac{1}{2}(\cos\left(\frac{\pi \cdot (\mathrm{CDF[i]})}{\max(\mathrm{CDF}) - \min(\mathrm{CDF})}\right) + 1) \tag{7.5}$$

With this result one has to calculate the effective $U_{(\text{eff LSB})} = \frac{u[N]-u[0]}{N}$ and then calculate the DNL using it's definition 7.1. The INL is calculated by fitting a linear function to the ADC response, and taking the difference between it and the measured values.

## 7.4. Results, Conclusion and Improvements

The resulting DNL and INL function are depicted in figure 7.4 and 7.5. The DNL seems to be of a reasonable value, never exceeding 1 LSB, which means that there are no missing codes. As visible, the INL measurement has two components to it: first the small saw-tooth structure originating from the internal ADC comparator architecture, and second, a global arc. With the INL measurement in figure 7.5, sine wave amplitude deviations on the order of 10ppm or -100dB the become visible. The global arc structure can be either an amplitude deviation of the input signal sine wave, an error of sine wave frequency, deviating from 7.3, or the INL of the ADC. If the equation 7.3 is not obeyed, the arc like structure increases to a point where the saw-tooth structure is rendered invisible.
This might lend itself to the conclusion that I made a slight experimental error while choosing the frequency $f_{sine}$, and the real integral nonlinearity is even smaller than depicted. As seen in the histogram in figure 7.3, the sine wave does not fill the whole ADC range from 0 .. $2^{14} - 1$. This is also the main point of improvement for a next measurement. As suggested by [8], it's required to slightly overdrive the ADC with a sine wave a little larger than the ADC can measure, to reduce the uncertainty, caused by the peaks in the ADC histogram.
Comparing the INL measurements with [13], the ADC used in the CAEN V1782 exhibits only one fifth of the integral nonlinearities. Using an appropriate ADC with small nonlinearities will greatly influence the differential $\beta$-spectrum and increase the chance of finding a sterile neutrino signature.

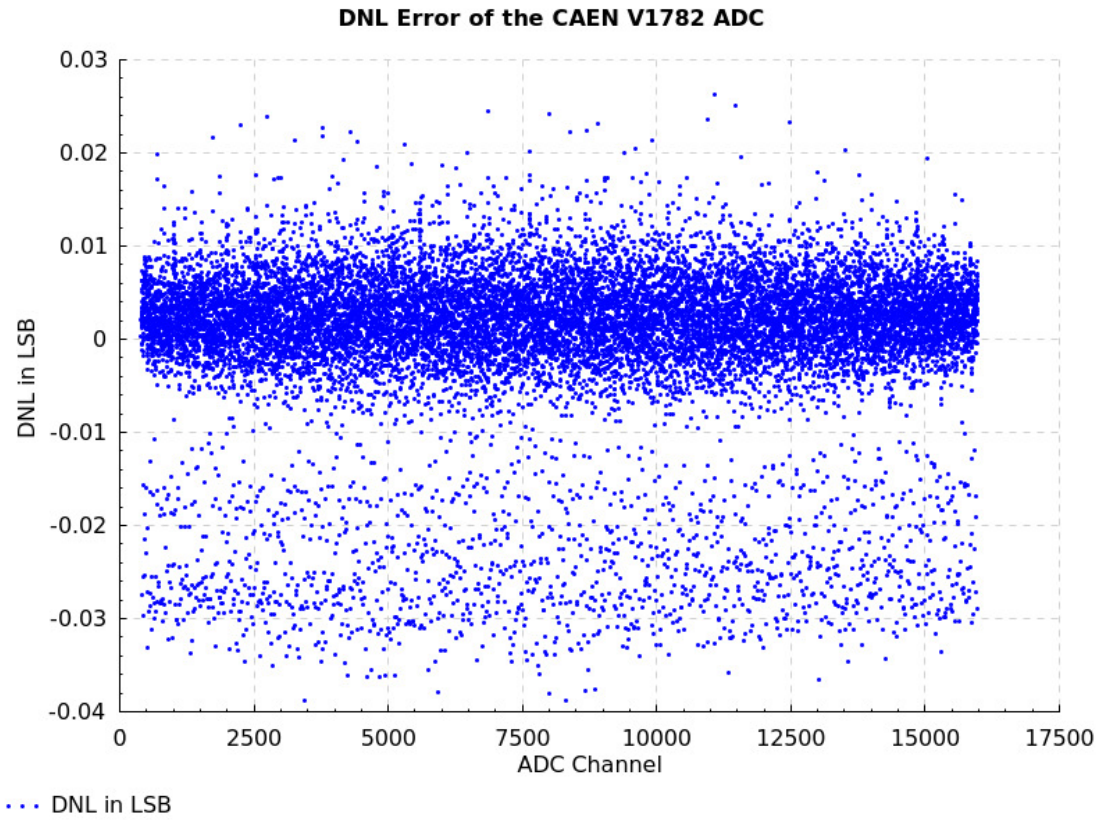



**Figure 7.4.:** The measured DNL of the CAEN V1782 ADC.

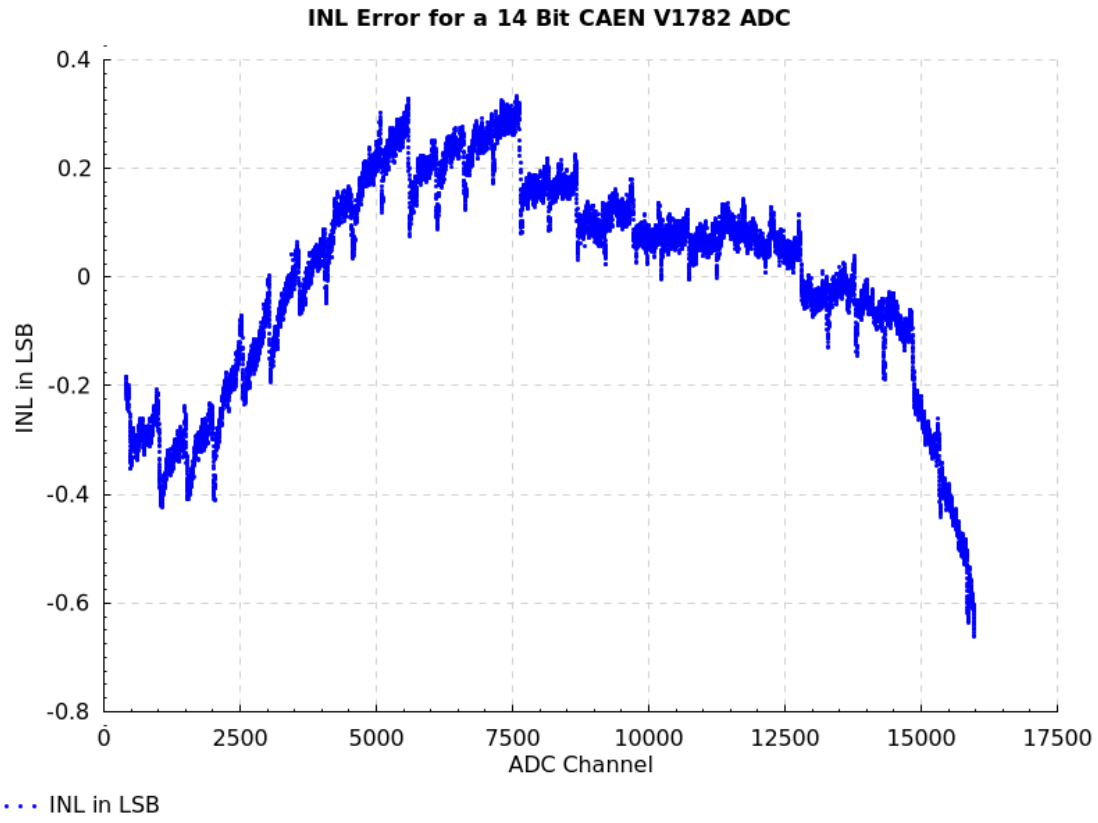



**Figure 7.5.:** The measured INL of the CAEN V1782 ADC.

# Chapter 8.

# Conclusion and Outlook

With the schematics that have been developed in this thesis, it's possible to achieve full detector operation. With minor modifications these schematics can be used on the planned tile main board, for the final TRISTAN design, enabling a search for the sterile neutrino in the near future. The performance results of the electronics are satisfying and the developed bias and buffer boards work to specification, I was able to operate the prototype 7 pixel TRISTAN detector, and compare it with the existing XGLAB setup. These measurements showed two main points of improvement: The high voltage linear regulator exhibits significant temperature dependence, which is caused by the gain controlling resistor divider in the circuit. Using a resistor divider, which is integrated onto one component, would minimize the problem, by reducing the temperature difference between the two resistors and the associated gain drift. The second point of improvement is the monitoring microcontroller ADC, which when operated, causes an oscillation on the bias board internal supply line. This oscillation propagates to the detector, reducing resolution. It can be removed by shutting down the ADC of the microcontroller.
With the newly developed 48 channel bias and buffer board , there is a promising prospect of a successful energy resolution measurement.
The documented ADC INL histogram measurement method has shown to be successful. The chapter can be used as a starting point for further measurements. When measuring these nonlinearities into the ppm level, it becomes blatantly clear, how precise the reference signal must be, as otherwise distortions creep in. For the final ADC specification setup, a very well filtered, pure sinewave needs to be used.

# Chapter 9.

# Acknowledgement

I would like to thank everyone for supporting me during the thesis, especially:

- Prof. Dr. Susanne Mertens for giving me this great opportunity to work on this fun electronics related topic in this exciting environment, and for being so patient with the measurement results.
- David Fink for the continuous and warm support with all electronics related question, and measurement setups.
- Korbinian Urban for helping me with the experimental setups for measuring the detector performance, the motivation to push through in hard times, the ice breaks and the fun table tennis games.
- Daniel Siegmann for magically fixing DANTE multiple times, the welcoming atmosphere and the permanent encouragement, if something failed.
- Sascha Wüstling for patient remote consulting with any electronic related questions.

and of course my girlfriend who enabled me to write this thesis with our daughter during the corona lockdown, my family and my friends for all the encouragement and immediate support.

# Appendix A.

# Appendix

### A.0.1. Simulation of the Sinking Linear Regulator

I simulated the schematic in figure A.1 with the simulation tool LTSpice. A 1mVpp (Vpp = voltage peak to peak) noise source simulates the worst case, which might get coupled in during real operation. The output voltage $U_{out}$ is viewed in figure 5.7. The simulation states, that the voltage is stable up to fluctuations of 600$\mu$V. As you saw . An important factor for stability in the simulation is the resistor (R12), in series with the filter capacitor (C2) at the output of the regulator. In real components, this series resistance occurs by construction.

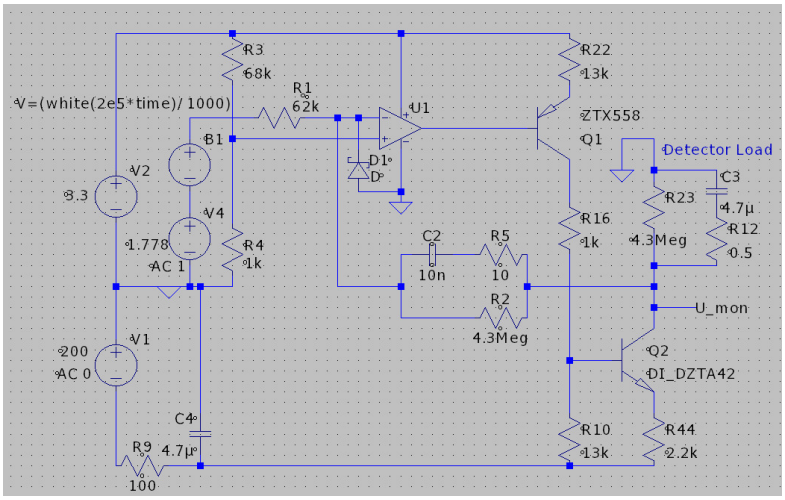



**Figure A.1.:** Simulated Linear Regulator with LTSpice

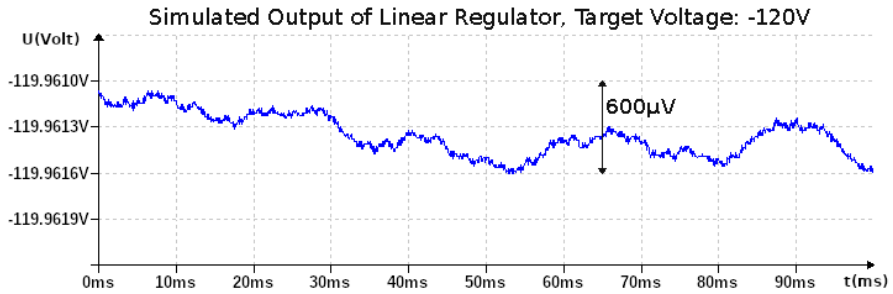



**Figure A.2.:** Output $U_{Out}$ of the linear regulator for a set-voltage of 120V. The approximate peak to peak voltage of the output is 600$\mu$V.

### A.0.2. Simulating the Stability of the Sinking Regulator

The output stability of the regulator importance. In order to improve the stability of the circuit, i added (C2) and (R5). This gives the OpAmp a faster response on AC signals, leaving DC properties unchanged. The lower ac impedance through (C2) is decisive for correct operation, as the transistors (Q1) and (Q2) operate in the nonlinear region, with the tendency to saturate. If that happens, the output of the regulator starts oscillating in a sawtooth shape. When omitting (C2), the sawtooth oscillation is visible in a transient analysis in time space, as shown in figure A.3. In the AC simulation, the phase shift required for a sinusoidal oscillation is not visible, due to the linearization of the transistor elements at the dc operating points.

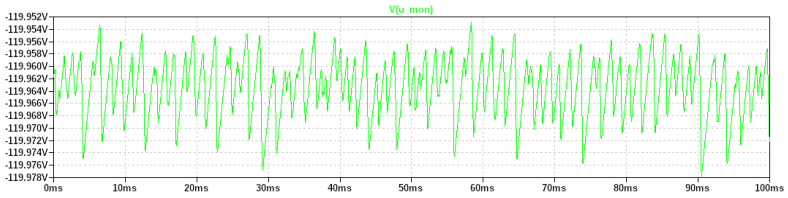



**Figure A.3.:** The output of the linear regulator, when the capacitor (C2) is omitted

### A.0.3. Simulation of the Sourcing Linear Regulator

Simulating the sourcing linear Regulator with a 1mVpp noise at the input shows a 800$\mu$Vpp noise at the output, as shown in figure A.4. The reason why the input noise does not get amplified by a factor of 70, is the feedback capacitor (C2).

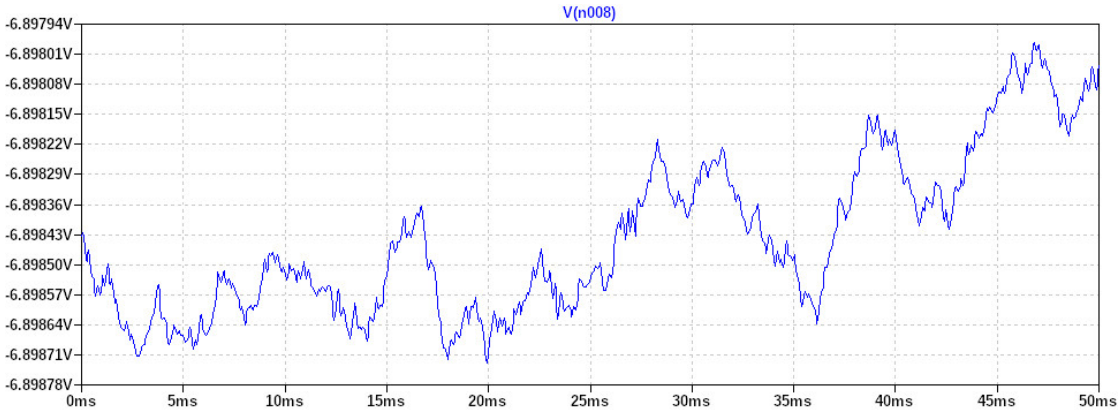



**Figure A.4.:** Simulated output of the souring linear regulator, as shown in figure 5.11. The visible amplitude of the noise is 800$\mu$Vpp, with a noise amplitude of 1mVpp at the input.

## A.1. Reset Generator

The reset generator supplies a rectangular pulse to flush off the charge from the detector anode. The pulse should go from -9V to +4V with a pulse-width of 200 nS to 5$\mu$S, and a frequency as low as several hundred hertz, and optionally as high as 500kHz. For experiment optimization purposes, the reset pulse should have an adjustable frequency, pulse-width and adjustable high and low levels. Furthermore, it must not output uncontrolled high voltages, whereas outputting a negative voltage is okay, as it only

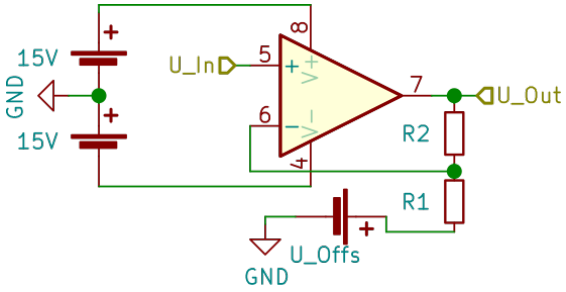



**Figure A.5.:** Basic Noninverting Amplifier

reverse biases the reset diode (D1) in figure 4.2 on page 12. The main part of the reset generator is a noninverting amplifier with an offset voltage, as shown in figure A.5. The gain of the amplifier is

$$G = 1 + \frac{R_2}{R_1}$$

and the output voltage

$$U_{\text{Out}} = G \cdot U_{\text{In}} + (G - 1) \cdot U_{\text{Offs}}$$

The function of resistor (R1) and the offset voltage $U_{\text{Offs}}$ from figure A.5, is fulfilled by the resistors (R9) and (R10), forming a Thevenin resistance of

$$R_1 \triangleq \frac{R_9 \cdot R_{10}}{R_9 + R_{10}}$$

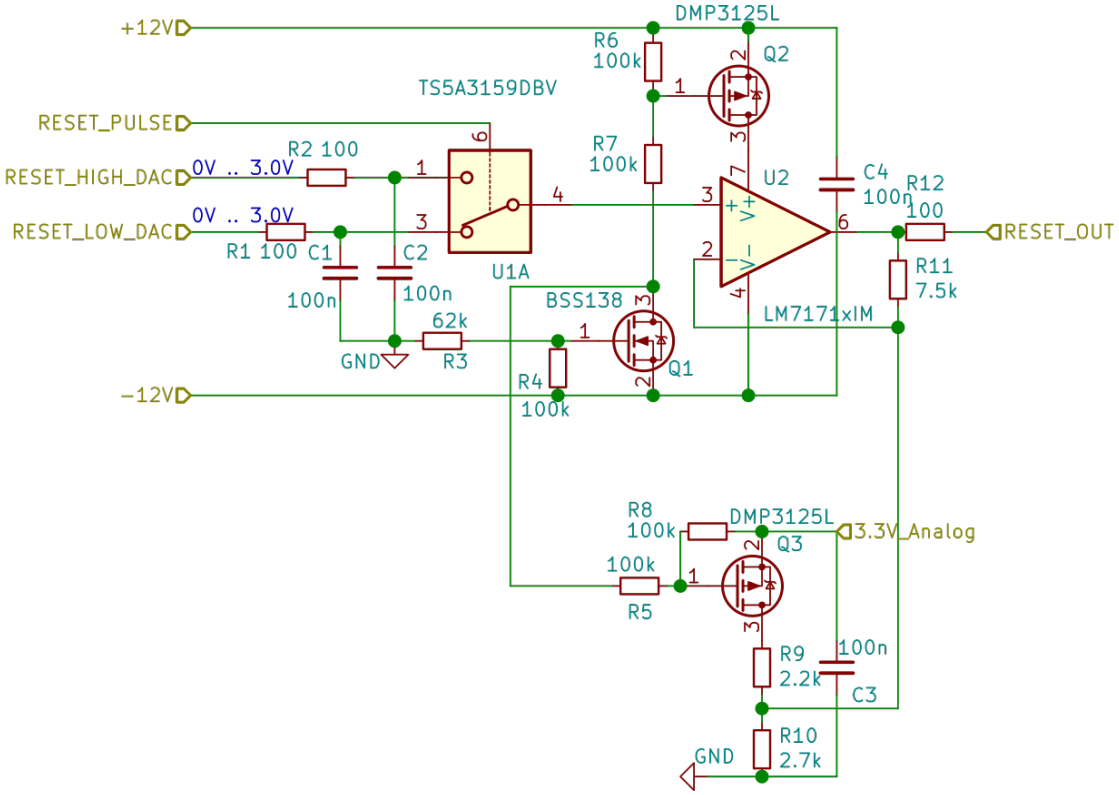



**Figure A.6.:** Adjustable reset pulse amplifier, with a 0 .. 3.3V reset pulse being generated by a microcontroller hardware timer.

to the offset potential

$$U_{\text{Offs}} = 3.3V \cdot \frac{R_{10}}{R_9 + R_{10}}$$

The transistors (Q1), (Q2) and (Q3) fulfill the function of blocking any positive uncontrolled voltages at the output. Only when the difference between the (GND) line and the (-12V) supply line reaches a threshold of 2.1V, transistors (Q2) and (Q3) start conducting current, supplying the OpAmp and the Thevenin resistor divider. This avoids positive voltages at the output, when the negative supply voltage is not present.
The value of 2.1V between (GND) line and (-12V) supply line arises from the gate-source threshold voltage $U_{GS(th)} = [\min(0.8V)..\max(1.5V)]$ of transistor (Q1), supplied by (R3) and (R4). Once

$$(GND) - (-12V) \geqq U_{GS(th)} \cdot \frac{(R_3 + R_4)}{R_4}$$

is reached, transistor (Q1) starts conducting current.
The amplifier input is switched between two DAC channels between 0 .. 3.0V by a microcontroller with the "RESET_PULSE" signal. The selected DAC voltage propagates to the amplifier input and gets amplified by a factor of

$$G = 1 + \frac{R_{11} \cdot (R_9 + R_{10})}{R_9 \cdot R_{10}}$$

, creating an adjustable reset generator.
It's important amplifier needs a sufficiently high internal bandwidth and a very high slew rate, in order to create pulses as high as 14V with risetimes lower than 50ns. The fidelity of the rectangular signal is secondary, as the signal is only used to pump away charge from the detector anode. The LM7171 is a fitting choice, being a high speed, high output current amplifier, with a datasheet slew rate of up to 4100V/$\mu$S and a high operating voltage of -15 to +15V.

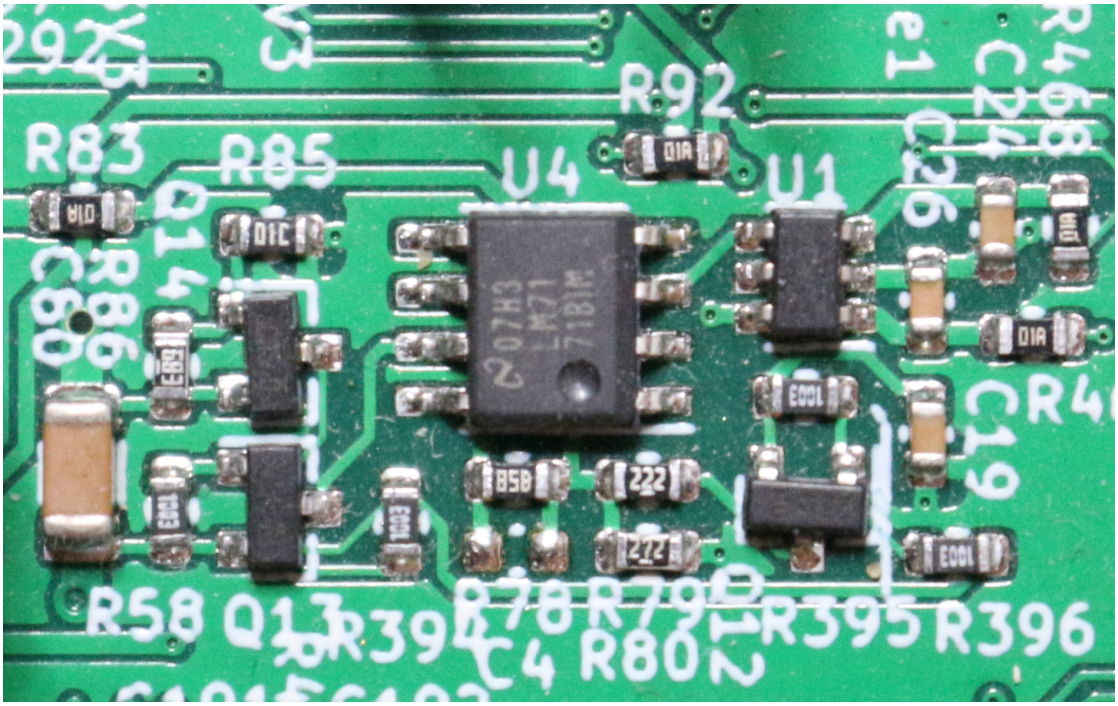



**Figure A.7.:** The reset circuit as drawn in schematic A.6

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